

Circuit Improvements to Q2LAL, S2LAL, and SCRL

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Abstract—This document identifies a circuit optimization for Static 2-Level Adiabatic Logic (S2LAL), Quiet 2-Level Adiabatic Logic (Q2LAL), and with some applicability to SCRL. When these logic families are used to create shift registers, about 30% of the transistors are redundant. The basic concept is explained, including how to eliminate the redundant transistors to reduce resource requirements without changing circuit function.

Keywords—*adiabatic computing; reversible computing; CMOS; cryo-CMOS; Static 2-Level Adiabatic Logic; S2LAL; Quiet 2-Level Adiabatic Logic; Q2LAL; Split-Rail Charge Recovery Logic*

I. BACKGROUND ON ADIABATIC LOGIC

This document is applicable to at least three existing adiabatic logic families, notably SCRL [1], S2LAL [2], and Q2LAL [3]. Interested readers are referred to the references.

II. REDUNDANT GATES

The observation is that when these logic families are used for shift registers, the resulting circuits will contain a sizable percentage of redundant transistors. Since shift registers can be used for data storage, applications with many shift registers may benefit by removal of the unnecessary transistors.

The observation and result are illustrated in Fig. 1.

Fig. 1a shows the reversible circuit framework that is the basis of SCRL, S2LAL, and Q2LAL.

Fig. 1b is the result of taking Fig. 1a and horizontally shifting the bottom row to the right until the transmission gates line up vertically. The reader will see that the adiabatic amplifiers (triangles) between adjacent pairs of transmission gates will have the same input and the same clock. It is further noted that the output of an adiabatic amplifier is determined only by its input—i. e. there is no tri-state output whose value is determined by an external source. This opens the possibility that such pairs of amplifiers could be merged, with the outputs of both such amplifiers connected together.

The previous statement requires that the adiabatic amplifiers have the same function and operate on the same data. For example, if F_4 was an AND function while R_2 was the XOR function, then merging the two amplifiers would change the circuit's function. However, the F's and R's in a shift register are either all inverters (SCRL) or all non-inverting

buffers (S2LAL and Q2LAL). Hence the merging will be valid for shift registers.

Fig 1c shows an alternative circuit geometry. The circuit shown in the same as Fig. 1b, but the crossovers are eliminated by flipping alternate stages upside down.

III. DISCUSSION

The advantage is a reduction in the number of transistors.

An S2LAL stage comprises two adiabatic amplifiers of 3 transistors each plus two transmission gates of 2 transistors each, for a total of 10 transistors. The simplification reduces the circuit to 7 transistors, a reduction of 30%

An Q2LAL stage [3] comprises two adiabatic amplifiers of 4 transistors each plus two transmission gates of 2 transistors each, for a total of 12 transistors. The simplification reduces the circuit to 8 transistors, a reduction of 1/3.

An SCRL stage [1] comprises two split-rail inverters of two transistors each plus two transmission gates of 2 transistors each, for a total of 8 transistors. This simplification reduces the circuit to 6 transistors, or a reduction of 25%. The SCRL circuits known to the author would need to have their clocking changed to accommodate this circuit simplification, so the change is less transparent than for the other families.

Since the method disclosed in this note is simply the elimination of redundant transistors, there will be no change in circuit function. This implies that the original circuit in Fig. 1a could be intermixed with the circuits in Fig. 1b or c. This would be appropriate for circuits that included logic, such as AND gates, intermixed with shift registers.

ACKNOWLEDGMENT

Michael P. Frank developed S2LAL and a consistent terminology [2], both of which became a starting point for this work. This document uses Mike's terminology, including diagrams, with his permission.

REFERENCES

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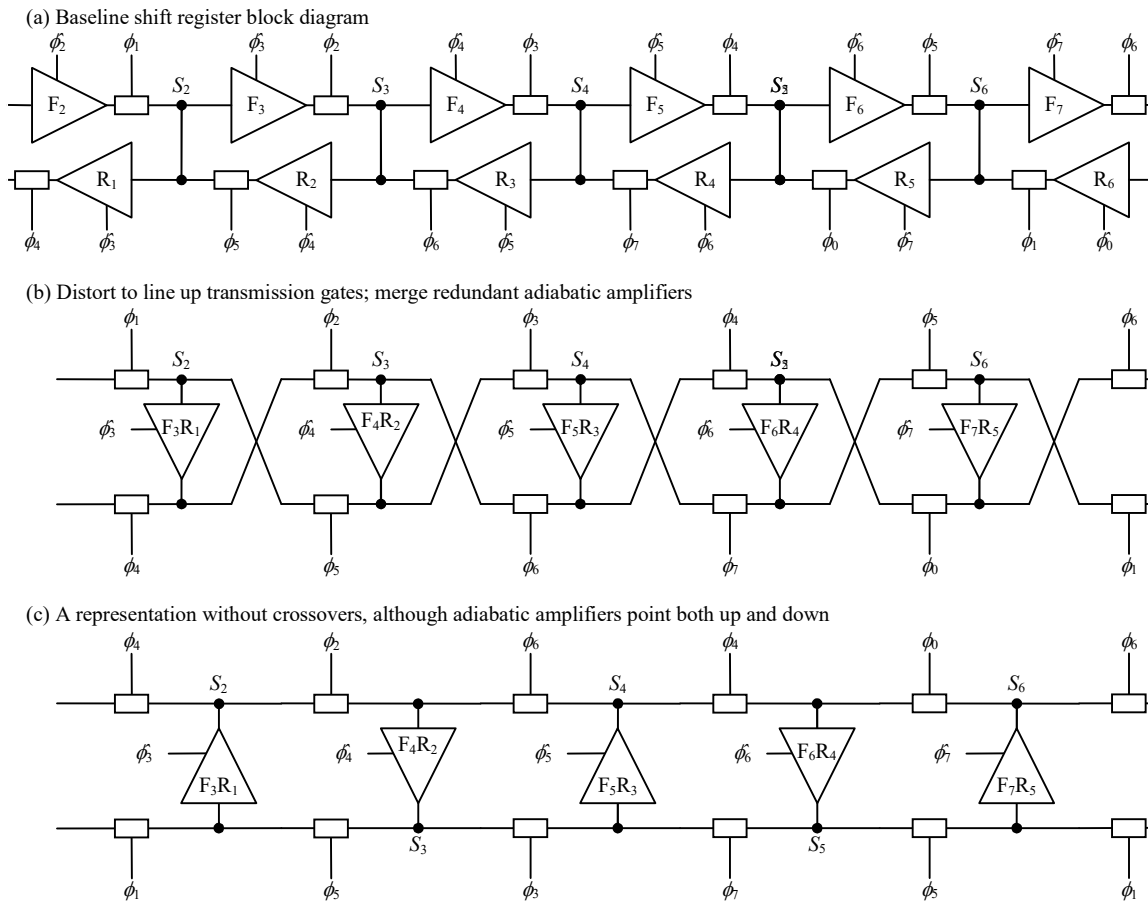


Fig. 1. Circuit simplification applicable to shift registers. (a) The familiar circuit diagram. (b) Shift the top row relative to the bottom row so the transmission gates line up. This will cause F_{n+2} to have the same inputs as R_n , so these circuits are redundant and merged, resulting in downward pointing triangle with labels $F_{n+2}R_n$. This is only valid if F_{n+2} the same function as R_n and the inputs are the same – which is true for shift registers. (c) If desired, the crossovers can be removed by vertically flipping every other stage.