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Rebooting Computing

An Audacious New Direction for Computing Hardware

Erik P. DeBenedictis¹

“Rebooting Computing” started in 2013 with the idea that a new computer architecture could restart Moore’s law. The search for a drop-in transistor replacement began and bore truly unexpected fruit. As no “quick fix” was found, state-of-the-art computation research splayed widely into everything from 3D packaging to analog neural networks on normal devices and quantum computers. We are already seeing powerful potentials from synergistically combining these disparate research lines. Here’s how they may develop.

There is a lot of research today on 3D chips and the integration of disparate technologies into the same package, but I see some audacious new ideas that could take this work beyond just packaging and make a fundamental advance in building computers.

Through-silicon vias (TSVs) are one of the best existing examples. These are modules comprised of up to, say, a half-dozen integrated circuit die interconnected electrically and mechanically with thousands of microscopic TSVs (bumps) along their planar faces. 3D flash is another example, where nearly 100 layers of memory devices are evaporatively deposited onto a CMOS integrated circuit base layer.

The unexpected advance I’m seeing is the extension of these approaches first to multiple operating temperatures, such as room temperature layers and other layers at one or more cryogenic temperatures. The cryogenic layers allow a second extension to novel devices and circuits, including both computing technology that is especially energy efficient at low temperatures and sensing devices that require specific temperatures to function.

This new approach is being applied outside the domain of microprocessors and memories. Microprocessors maximize the computational throughput of each transistor. In spite of the microprocessor being the visible architecture of the current era, most transistors are actually used in memory or storage, where their job hold data without change. The new approach I’m seeing is being applied as support functions for sensor arrays or proposed for quantum computer control electronics. Devices in these new systems are not divided into logic and memory in the traditional way, and the throughput of the logic is not on the critical path to delivering value to the user. This implies a deep change in design objectives.

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Logic performance and temperature

There was an extensive search for an alternative to the transistor, leading to the scatter plot in figure 1 of energy and delay for many devices.¹ However, there are three additional light-blue solid dots for cryogenic Josephson junction-based Reciprocal Quantum Logic (RQL) and Adiabatic Quantum Flux Parametron (AQFP) circuits. The “whiskers” show the sum of device dissipation plus the energy of the cryogenic refrigerator that removes the device’s heat from 4K to room temperature, over a typical refrigerator efficiency range. None of the devices stand out.

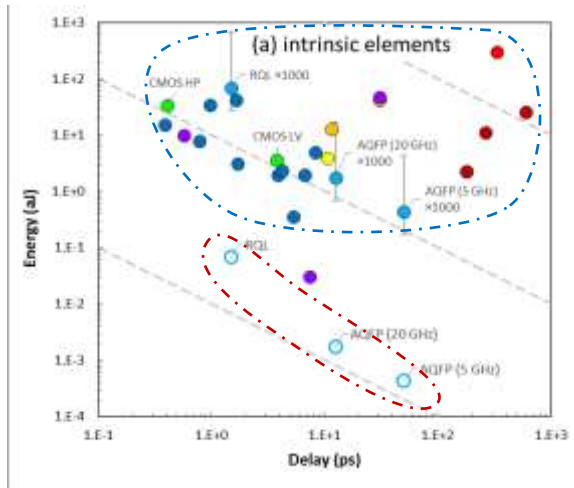


Figure 1. An energy-delay plot of a comprehensive set of logic devices at room temperature, yet including Josephson junctions operating at 4K in three circuits (RQL and AQFP at two speeds). None of the devices stand out at room temperature because only the superconducting ones have refrigeration overhead. However, at 4K they all require refrigeration, causing the superconducting devices to stand out. (The outlier purple dot is a BisFET, which is too immature to be taken as a serious contender.)

When low temperature operation is required, all the devices in figure 1 need refrigeration. This changes the accounting of cryogenic refrigeration energy. In low-temperature operation, both the upper and lower groups represent devices operating at temperature T and where a cryogenic refrigerator must remove heat to room temperature. The refrigerator will ultimately multiply the heat by $300K/T$ in the process of moving it to the room temperature (300K) environment—assuming the refrigerator is 100% Carnot efficient. Refrigerator inefficiency adds another multiple of 5-20 \times to this heat, yet equally for all the situations covered by this article. The Josephson junction-based devices stand out.

Different circuits become effective at low temperatures

Everybody wants to save energy, which is why wise engineers consider energy efficient light bulbs for their homes. Once they see that the energy efficient bulb costs \$4 instead of 50¢ for an incandescent one, they do a calculation to see if it’s a good deal. How much does the increased purchase price offset the energy savings over the bulb’s lifetime? Energy

savings technology, such as reversible and adiabatic logic, have been known for years. Unfortunately, they trade energy efficiency during operation for more complex circuits that cost more to buy in the first place—leading to the same tradeoff as light bulbs.

Other things being equal, you become more likely to choose the energy efficient technology as the price of energy rises. Energy efficient lights or reversible computing that are bad deals at room temperature may become a good deal at 4K due to the effective 1000× increase in energy cost—and an even better deal for a cryogenic telescope or quantum computer operating a millikelvins where the overhead is 1M×.

Adiabatic and reversible logic have been studied at room temperature from many years, with the base plot in figure 2 showing its benefit when implemented with standard CMOS. The curves are the result of many simulations and show transistor power declining with operating frequency for both standard CMOS and a reversible logic circuit called 2LAL. However, all the curves eventually level out due to leakage current I_{off} .

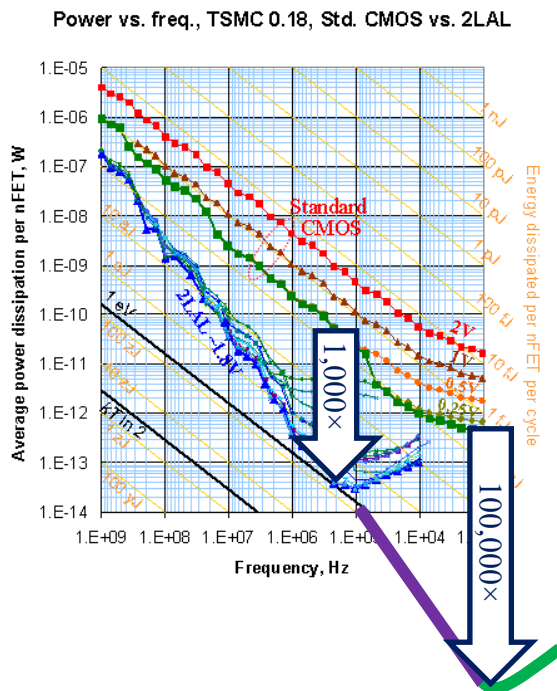


Figure 2. Comparison of circuit efficiency for standard CMOS (top) and a reversible circuit 2LAL, showing a maximum advantage of 1000× at 200kHz. However, if 2LAL is operated at 4K, down sloping curves should extend further, leading to a possible 100,000× energy efficiency improvement over room temperature electronics. This may allow transistorized 2LAL to compete with Josephson junctions in applications where speed is not essential.

Standard CMOS declines with slope -1 (linear) while 2LAL has slope -2 (quadratic). This creates a widening advantage for 2LAL as operating frequency declines. However, nobody wants a microprocessor with more complex circuits that runs at 200kHz—even if it is energy efficient.

What happens to reversible circuits at cryogenic temperatures? Studies of standard CMOS transistors operated at 4K show a reduction in leakage current,² but other factors are nearly unchanged. While cryogenic 2LAL has not been systematically analyzed for this article, the qualitative result should be extension of the region with downward slope -2 by

an additional factor of perhaps 10,000× before I_{off} static leakage causes the upward sloping behavior. A review of the literature indicates the advantage should increase a bit further below 4K and then level off, but further work is indicated.

Superconductor electronics was set aside long ago as not interesting, but the “end of Moore’s law” changed design criteria so superconductors can beat semiconductors. But in a last minute reversal, semiconductors catch up again by using reversible computing circuits that had long ago been discarded. What if semiconductors and superconductors could work together?

Heterogeneous integration of semiconductors and superconductors

I saw a presentation at a recent conference reporting on the invention of a superconducting field-effect transistor. It was kind of an odd device. Through application of 90V, it would switch from a 0Ω superconductor into a resistor of 50Ω or so. Nobody had any idea what to do with it, but I’ll offer the suggestion that it could interface between semiconductors and superconductors in a hybrid module.

While the device was experimentally tested with 90V swings, the authors claim scaling could reduce the drive voltage to 2.5V, a typical CMOS voltage swing. This could lead to a structure like shown in Figure 3, where CMOS voltage signals are converted to Josephson junction current signals.

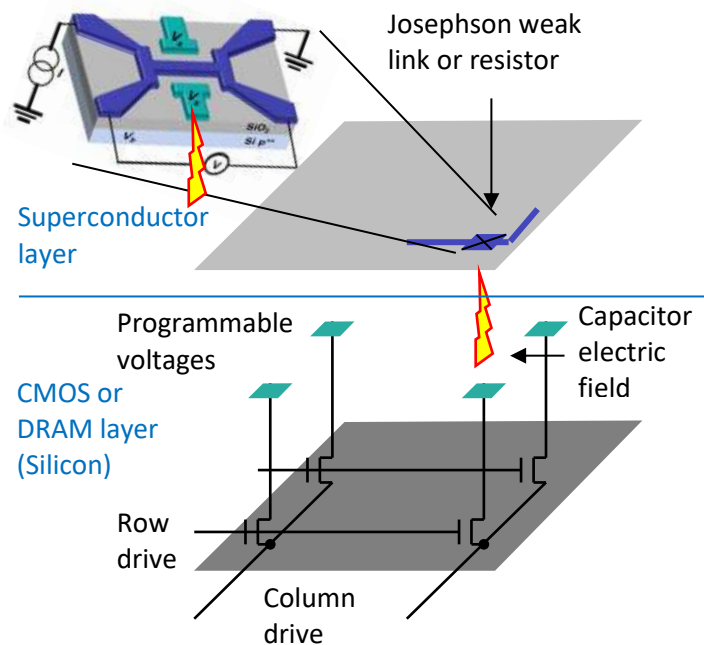


Figure 3. A possible semiconductor-superconductor hybrid. The semiconductor layer applies voltage-based signals to the gates of superconducting FETs, which translate the signals into a form readily used by superconducting circuits. The hybrid would be fabricated by using a CMOS wafer as a base for depositing superconductor circuits—in

lieu of today's method of using a blank Silicon wafer as a base.

The inset in figure 3 shows a superconducting FET.³ Ignoring the green structures for the moment, the blue structure is a superconducting wire that will conduct current horizontally with zero resistance. However, a narrow superconducting wire only conducts with zero resistance up to a maximum current, called the critical current, above which the device becomes a resistor. A narrow wire of this type is called a weak link and is a variant of a Josephson junction.

Superconductivity can be disrupted by an electric field, such as the field applied by the green capacitor plate in figure 3 and the green structure in the inset. Theory and experiment for the superconducting FET show the weak link's critical current changes when the green structure applies voltage of a few volts or more, positive or negative.

The semiconductor layer could communicate with the superconducting layer through changes in critical current.

Attempts to restore traditional computer performance growth rates, essentially Moore's law, splayed into different directions.

For example, there has been extensive R&D on boxes filled with superconductor electronics running at 4K or colder connected to a box of semiconductor electronics at room temperature (both cryogenic supercomputers and superconducting qubit quantum computers fit this description). After all, who would want to run semiconductors at 4K when it wasn't absolutely necessary?

We've seen how these directions can be deployed at the same time to make a more audacious hybrid than has been seen before. Running both semiconductors and superconductors at cryogenic temperatures, with an efficient interface between the two, yields a set of building blocks with a unique set of properties:

- Semiconductors: Large number of components per unit area and high maturity. Signals have 1-2V swings. However, achieving high energy efficiency requires progressively reducing the clock rate.
- Superconductors: Clock rate remains high down to low temperatures, but these immature devices have large features that would result in low device density. Signal voltages are around a millivolt.

Is there any circuit in common use that would benefit from such an odd-ball combination of features? My first thought is a superconducting FPGA,^{4,5} where the configuration logic is built from semiconductor. Configuration is only performed on power-up, so it doesn't matter if it runs slowly. After this FPGA has been configured, the Josephson junction logic executes the programmed function at high speed.

There could be many other applications, such as exotic sensor processing arrays for astronomy and quantum computer control electronics—but these will be a topic for future development.

References

1. Nikonov, Dmitri E., and Ian A. Young. "Overview of beyond-CMOS devices and a uniform methodology for their benchmarking." *Proceedings of the IEEE* 101.12 (2013): 2498-2533.

2. Incandela, Rosario M., et al. "Characterization and Compact Modeling of Nanometer CMOS Transistors at Deep-Cryogenic Temperatures." *IEEE Journal of the Electron Devices Society* (2018).
3. De Simoni, Giorgio, et al. "Metallic supercurrent field-effect transistor." *Nature nanotechnology* (2018): 1. <https://doi.org/10.1038/s41565-018-0190-3> <https://arxiv.org/pdf/1710.02400>
<https://www.nature.com/articles/s41565-018-0190-3.pdf?origin=ppub>
4. Fourie, Coenrad J., and Hein van Heerden. "An RSFQ superconductive programmable gate array." *IEEE Transactions on Applied Superconductivity* 17.2 (2007): 538-541. <https://doi.org/10.1109/TASC.2007.897387>
5. Katam, Naveen Kumar, Oleg A. Mukhanov, and Massoud Pedram. "Superconducting magnetic field programmable gate array." *IEEE Transactions on Applied Superconductivity* 28.2 (2018): 1-12. <https://doi.org/10.1109/TASC.2018.2797262>

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