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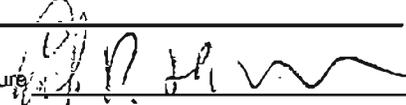
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## The Sandia Petaflops Planner

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### Abstract

The Sandia Petaflops Planner is a tool for projecting the design and performance of parallel supercomputers into the future. The mathematical basis of these projections is the International Technology Roadmap for Semiconductors (ITRS, or a detailed version of Moore's Law) and DOE balance factors for supercomputer procurements. The planner is capable of various forms of scenario analysis, cost estimation, and technology analysis. The tool is described along with technology conclusions regarding PFLOPS-level supercomputers in the upcoming decade.

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The Sandia Petaflops Planner is a tool for projecting the design and performance of parallel supercomputers into the future. The mathematical basis of these projections is the International Technology Roadmap for Semiconductors (ITRS, or a detailed version of Moore's Law) and DOE balance factors for supercomputer procurements. The planner is capable of various forms of scenario analysis, cost estimation, and technology analysis. The tool is described along with technology conclusions regarding PFLOPS-level supercomputers in the upcoming decade.

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## Nomenclature

ASCI.....	Advanced Simulation and Computing (the “I” is silent)
ASIC.....	Application Specific Integrated Circuit
DOE.....	Department of Energy
DRAM.....	Dynamic Random Access Memory
FLOPS.....	Floating Operations Per Second
GFLOPS.....	$10^9$ Floating Operations per Second
IPC IO.....	Interprocessor Communications Input Output (I. e. MPI)
ITRS.....	International Technology Roadmap for Semiconductors
MPI.....	Message Passing Interface
MPP.....	Massively Parallel Processor
MPU.....	MicroProcessor Unit
PetaFLOPS.....	$10^{15}$ Floating Operations Per Second
PIM.....	Processor In Memory
SNL.....	Sandia National Laboratories
TFLOPS.....	$10^{12}$ Floating Operations Per Second

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## **Introduction**

Over the past 20 years, parallel supercomputers have gone from an academic curiosity to vital tools for science, defense, engineering, and a host of other fields. The Department of Energy's (DOE's) Advanced Simulation and Computing (ASCI) program has driven the development of parallel supercomputers through a staged series of procurements up to the current programmatic limit of 100 TFLOPS. It seems evident that applications will continue to want more power, causing us to wonder if the computer technology is up to the task?

To answer this, we need to find an oracle to foretell the future of supercomputers. We found our oracle in Moore's Law, or more specifically the extensive body of knowledge known as the ITRS roadmap developed by the semiconductor industry projecting future progress in integrated circuits. To apply Moore's Law for integrated circuits to supercomputers, we need an abstracted definition of a supercomputer that can be applied to hypothetical supercomputers in the future. We found this definition in the procurement rules for DOE supercomputers. Over the half-dozen generations of DOE supercomputer procurements, DOE labs have figured out how to specify the relationships between a supercomputer's computing rate, memory size, communications rate, etc. needed for a machine to work well for applications. Adding Moore's Law to DOE's procurement rules yields hundreds of parameters and mathematical relationships – but which can be solved with effort.

We wrote a "Petaflops Planner" program that essentially projects popular supercomputer designs into the future using Moore's Law. We wrote the planner as a tool for multiple purposes: testing hypotheses on computer architecture, optimizing designs, projecting costs, etc.

We then used the planner to see if computer technology was up to the task of PFLOPS-level supercomputers. The body of the paper explains how the answer can be "yes," but only by employing new technology.

## **Previous Work**

### **Balance factors**

Sandia and other DOE laboratories have had criteria for specifying supercomputers in procurements. These criteria have been applied to supercomputers with vastly different performance levels over the last 20 years. As a result, the criteria have become scalable rules that define supercomputers that will perform well within the DOE.

	DATA-INTENSIVE (RED STORM <sup>1</sup> )	COMPUTE-INTENSIVE (PURPLE <sup>2</sup> )
Memory Bytes/FLOP	1.0 TFLOPS <sup>-25</sup>	1.0 TFLOPS <sup>-25</sup>
Memory Bandwidth Bytes/FLOP	4	1
Peak IPC IO Bytes/sec/FLOP	2	.1/12.≈.01
Total IPC IO Bytes/sec/FLOP	2	.1
Network bisection bandwidth Bytes/sec/FLOP	.075	.05

Table 1: Balance Factors

These scalable rules are based on “balance factors”<sup>[ref 1, 2]</sup>. A DOE laboratory begins by specifying a performance target – originally measured as peak GFLOPS, now peak TFLOPS. The balance factors specify the values of other parameters as a function of the peak FLOPS. DOE procurements tend to use similar balance factors, but with different values representing a different application mix (table 1).

### Architectures and Packaging Styles

The supercomputing community has just a few leading architectures or design styles:

- Virtually all supercomputer today are clusters of Symmetric MultiProcessors (SMPs, figure 1), which are composed of separate commodity microprocessor chips, memory chips, and a router implemented as an Application Specific Integrated Circuit (ASIC).



Figure 1: An SMP Node

- nCUBE Corporation pioneered a different implementation style where the CPU and router are both in the same ASIC chip, but with separate memory (figure 2). IBM is using this implementation style for the DOE Blue Light project.

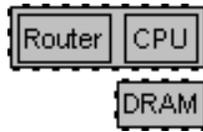


Figure 2: An nCUBE Node

- Processor-In-Memory (PIM) represents a more radical departure. PIMs include processors, memory, and router in a single chip – often hundreds of each (figure 3). PIM systems may consist of homogeneous arrays of PIM chips, but may also include additional conventional memory. There are different views on the best “instruction set” for PIMs, and some designs may represent a different architecture as well as a different packaging style.

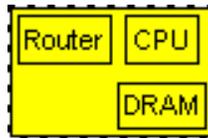


Figure 3: A PIM Node

## Semiconductor Roadmap

The ITRS roadmap<sup>[ref. 3]</sup> is a project by the semiconductor industry to track the progress of semiconductor technology, identifying roadblocks before they become problems. While Moore’s Law is a one-sentence statement, the ITRS Roadmap is a time comparable in size to a telephone book (figure 4).

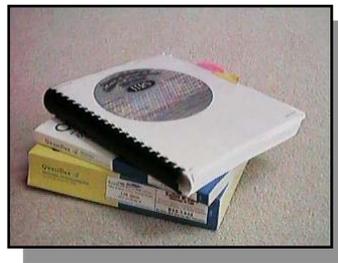


Figure 4: The ITRS compared to the Albuquerque Telephone Book

A sample from the 1999 ITRS roadmap illustrates the process. The Semiconductor Industries Association (SIA) establishes a panel of experts in each of about a dozen aspects of semiconductor technology (process technology, packaging, DRAM design, testing, ...). These experts analyze progress in their area, either confirming that Moore’s Law can be maintained or identifying obstacles. To fit on the printed page, each table comes in a near term and long term part (figure 5). Each technology item is designated white, yellow,

or red depending on the state of known technology. As illustrated (figure 5), assembly and packaging are areas of concern in 1999.

Table 59b *Assembly & Packaging Technology Requirements—Long Term (continued)*

YEAR TECHNOLOGY NODE	2008 70 nm	2011 50 nm	2014 35 nm
<i>Performance: On-Chip (MHz) [E]</i>			
Low cost	840	1044	1250
Hand-held	840	1044	1250
Cost-performance	1400	1800	2200
High-performance	2500	3000	3600
Harsh	100	100	100
Memory (D/SRAM)	175/700	200/900	225/1100
<i>Performance: Chip-to-Board for Peripheral Buses (MHz)</i>			
Low cost	125	125	150
Hand-held	125	125	150
Cost-performance [F]	175/700	200/900	225/1100
High-performance [G]	1250	1500	1800
Harsh	100	100	125
Memory (D/SRAM) [F]	175/700	200/900	225/1100

Solutions Exist



Solutions Being Pursued



No Known Solutions



Figure 5: Example Chart from ITRS

## The Petaflops Planner

### Abstract Supercomputer Representation

The planner represents a supercomputer as a collection of SMP nodes. Each node is comprised of chips defined by Silicon area and pin count. The wires connect the pins. The planner then calculates system performance assuming the system is assembled according to one of the architectures described above. The planner assumes each chip, pin, and wire will perform to its maximum capacity. System cost is computed by using ITRS cost figures for ASICs, MPUs, DRAMS, etc.

The illustration of a PIM (figure 6) illustrates the planner's level of abstraction. The rectangle is displayed of a size proportional to the chip area. The yellow area represents RAM on a PIM and blue and red represent processor cores, with the amount of each color proportional to the Silicon area consumed by the component. The planner deals only with area, not specific circuitry.

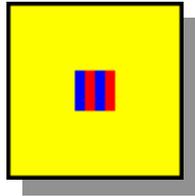


Figure 6: PIM Chip Layout Model

## Interconnect

The Petaflops Planner assumes a 3-d mesh topology. The rationale is as follows:

- By choosing a 3-d mesh topology, we trivialize analysis of the mapping between the supercomputer topology and the topology of the machine room. All machine rooms in the universe are 3-d, because the universe is 3-d (spatially). Thus, we can put a 3-d supercomputer into a machine room without having any long wires. The “fat tree” is other popular interconnect topology. Putting a “fat tree” supercomputer into a 3-d machine room involves a spatial mapping and some long wires. Long wires introduce both cost and delay.
- Sandia National Laboratories (SNL) has a history of procuring 3-d mesh supercomputers that remain the “fastest computer on earth” longer than anybody expects. Hence, there is no evidence of a performance penalty by limiting the analysis to 3-d meshes.

## Derated Flops

The planner uses a method we call “derated flops” to calculate system performance. The rationale is as follows: Imagine that system performance was based solely on peak FLOPS, and that we would use an architectural optimization method (as we do). With peak FLOPS as the objective function, an optimizer would be expected to find systems where the chips were packed solid with floating point units. These systems would not perform well on real applications because they would lack memory and IPC IO. We found that by “derating” the flop rate so that balance was preserved, we got an objective function suitable for optimization.

We define the “derated flops” for a system as the maximum number of FLOPS that can be claimed while still meeting the balance factors. For example, say the balance factors call for one byte of memory bandwidth per flop. A microprocessor with 10 GFLOPS floating performance and 1 gbyte/second memory bandwidth would therefore be unbalanced. However, we permit the vendor to claim a “derated flops” rate of 1 GFLOP for the microprocessor. One GFLOP is the

highest flop rate that could be claimed without violating the balance factor for memory bandwidth.

## **Other Factors**

We considered two other factors in designing the planner:

Technology derating factor. Observers have long noticed that industry puts the best technology into consumer and commercial products where volumes and profits are highest. Supercomputing tends to get technology a couple years later. To capture this behavior, the planner lets the user specify a “technology derating factor.” Certain ITRS projections get multiplied by this factor to model this delay. The figures that get cut include ASIC density and clock rate, but do not include commodity microprocessor performance and memory density (because supercomputers can include the latest commodity components).

Power. The planner calculates power consumption, but does not use it as a constraint. The calculation applies CMOS power scaling rules to typical values for today’s microprocessors and memories. (It would be desirable for the planner to know maximum power dissipation per chip and then stop allocating components when that power has been reached.)

## **Architectural Optimization**

The planner can optimize designs. The architectural alternatives being considered are parameterized by one or two integers representing the number of CPU cores or memory chips. The planner picks the optimal value(s) for these parameters by iterating over all reasonable values of these integers and noting the value producing the lowest cost per derated flops ratio.

## **Implementation**

We constructed the Petaflops Planner to implement the design process described above. The planner was written in C++ for Windows and Linux and acts as an Internet Web server. That is, the planner starts and listens on a TCP/IP port for Web page accesses from a browser. A user accessing the planner via a browser sees a small Web site with help files, forms for specifying balance factors, and dynamic pages representing candidate supercomputers.

The diagram (figure 7) shows the Web form where the user specifies balance factors.

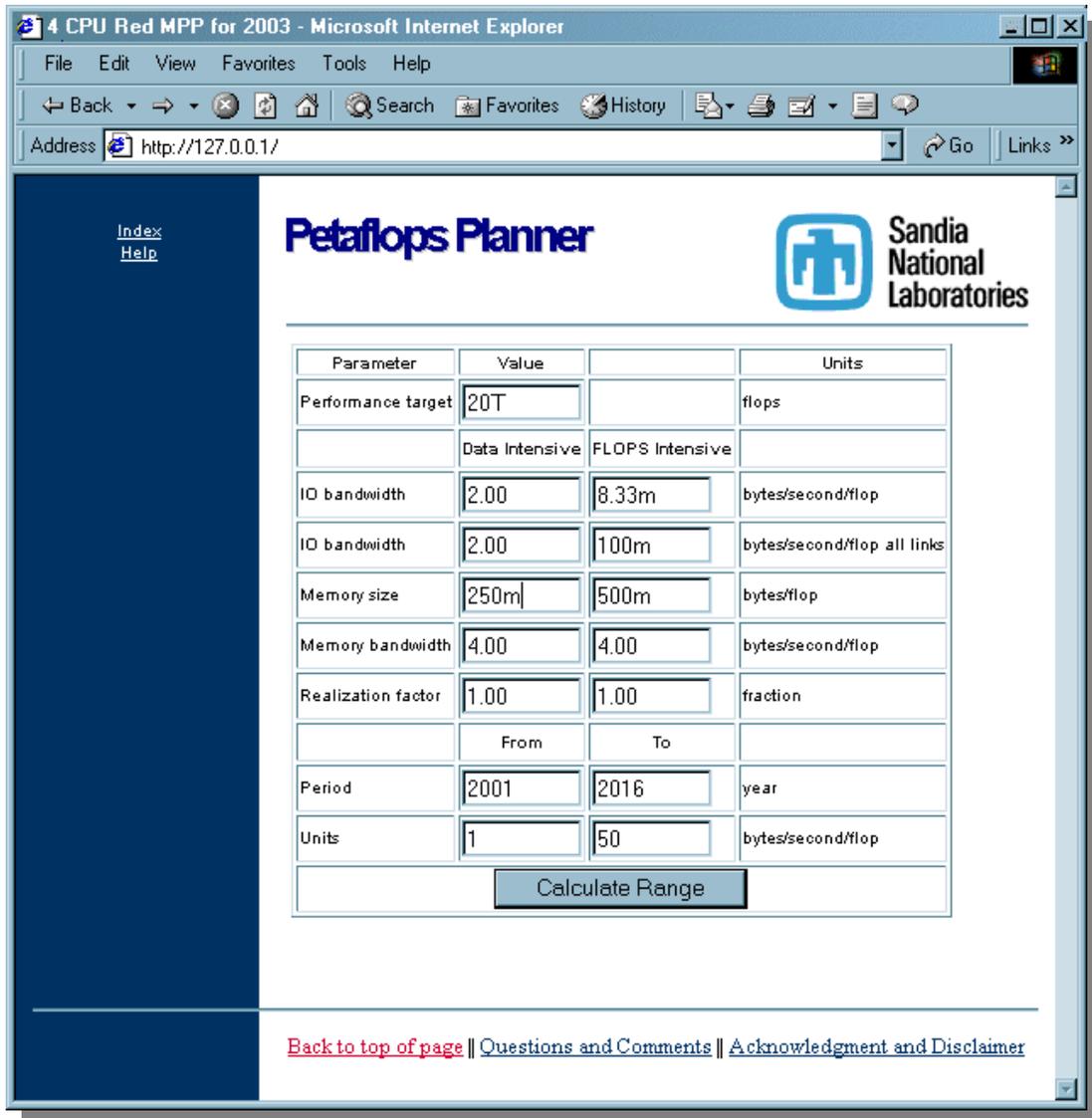


Figure 7: Petaflops Planner Input Form

Upon receiving balance factors, the planner computes several dozen optimal designs and provides a table of hyperlinks for details on each design. The table (not shown) has rows corresponding to year within the range of the ITRS projections and columns corresponding to four candidate architectures and packaging styles. The values in the table cells report the optimal number of CPU cores for the designated architecture in the designated year. Clicking on the hyperlink in the table cell yields a detail page for the design.

The diagram (figure 8) shows a detail page. The planner shows a diagram of a node board, scaling the squares representing chips proportionally to the necessary chip area. The parameters (size, power dissipation, memory capacity)

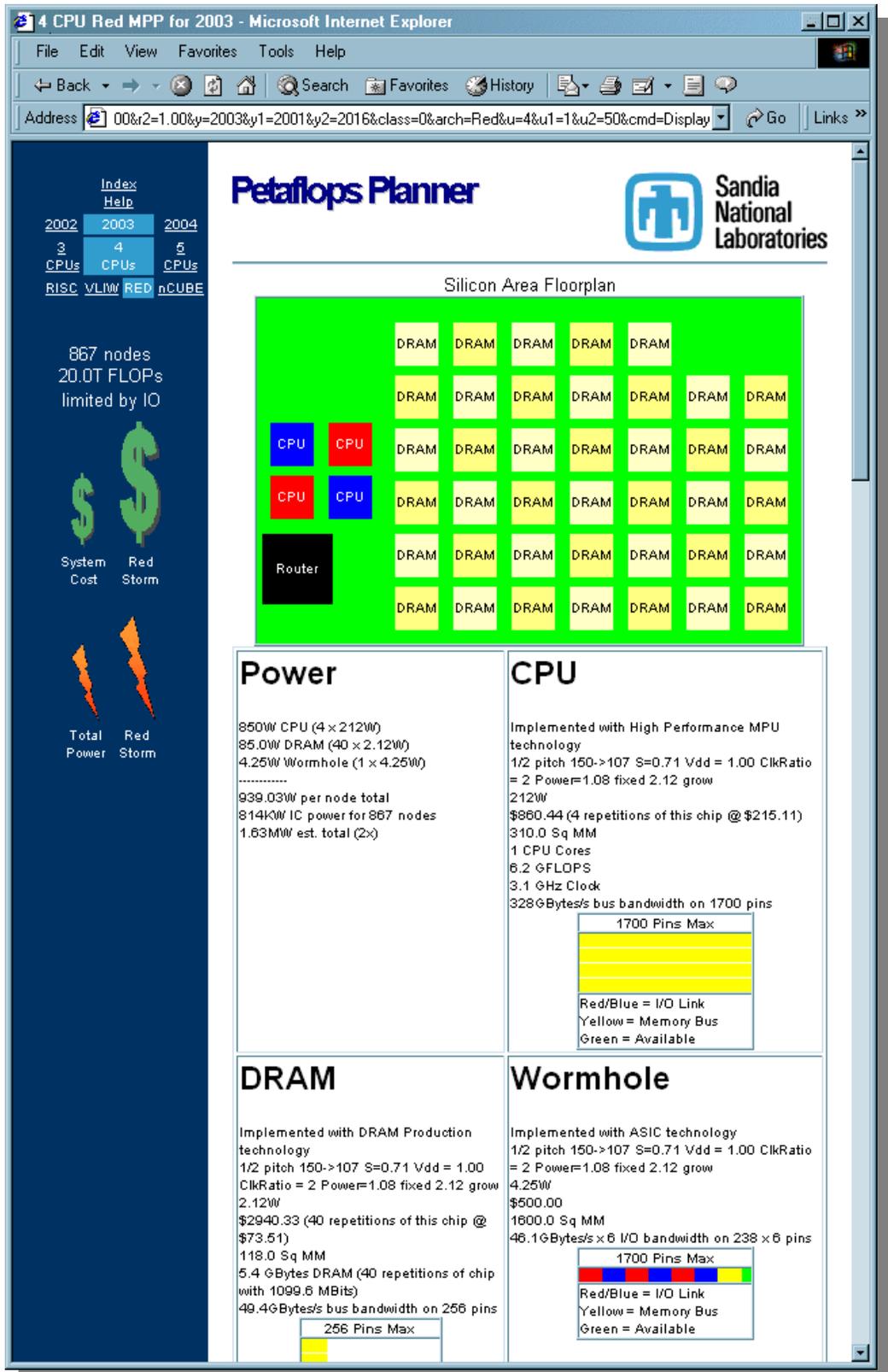


Figure 8: Petaflops Planner Output Page

of each type are reported textually. A bar graph shows the maximum number of pins on a chip and their allocation. The upper-right of the Web page includes a navigation panel that will display detail pages for designs in other years, architectures, and numbers of processors.

## **Results of Using the Petaflops Planner**

### **The Tool Worked**

We have had no problems with stability of the optimization algorithm. Furthermore, we've reviewed the planner's output with various people at Sandia and the results appeared plausible. The tool's speed is acceptable: a 266 MHz PC takes about 2 seconds to perform the ~10,000 design evaluations resulting from submitting balance parameters.

### **Moore's Law Holds**

We wanted to know if supercomputer performance would continue to increase at historical rates to the PFLOPS level. To do this, we calculated and plotted (on a log scale) the estimated cost for an optimal 5 PFLOPS supercomputer for each year into the future and for all the architectures. We expected to see one of two behaviors, both represented in the graph (figure 9):

- Straight lines sloping downward, representing continuation of the exponential progress of Moore's Law.
- Lines that slope downwards for while, followed by a leveling off. This would be the expected result if there were a critical, non-scalable technology component: as other technology components pass it by, the non-scalable component dominates the cost.

As shown in the graph, the planner found both behaviors. The shorter lines (ending in 2014) are based on the 1999 ITRS projections and predict failure of Moore's Law, whereas the longer lines (ending in 2016) are based on 2000 ITRS projections and predict continuation of Moore's Law. This discrepancy is described further below.

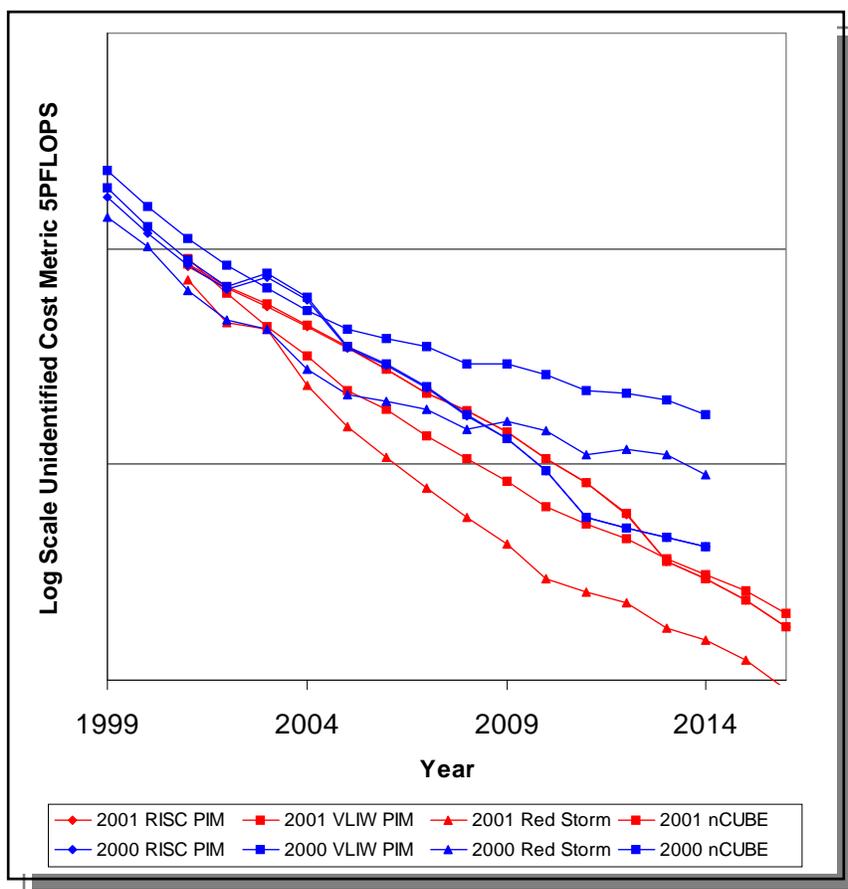


Figure 9: Architecture Costs

### Wires and LVDS

The change in conclusion between projections based on 1999 and 2000 ITRS tables illustrates the power and limitations of our approach.

In late 2001 we ran the analysis with the then-current ITRS 1999 tables and were alarmed at the apparent failure of Moore's Law. Examining the optimized designs in the later years revealed enormous chips with thousands of pins with IPC IO busses between chips hundreds of pins wide. Even with such enormous resources applied to chip-to-chip communications, the cores of the chips were "starved" for data. The pertinent ITRS table (figure 5) confirmed the problem: the speed of chip-to-chip communications via pins is limited to several gigabits/second/wire, and the maximum number of pins on a chip is not scaling with Moore's Law. Apparently supercomputers require chip-to-chip bandwidth beyond the scalability of pin-and-wire technology, and as a result Moore's Law fails.

When we ran the planner in early 2002 with the new ITRS 2001 tables, the problem went away. Between 1999 and 2000, a new type of chip-to-chip signaling technology reached the threshold of acceptance and was incorporated into the ITRS 2000 tables. The new technology was Low Voltage Differential Signaling (LVDS, right). Instead of using one wire per bit, LVDS uses two wires driven differentially (+V and -V). The signals are detected by differential amplifiers, where electrical noise cancels. This permits reliable signal recovery at lower power and at higher speed. While LVDS uses twice the pins and wires, the transmission rate becomes scalable with Moore's law. A regular wire is limited to 1 gbit/second whereas a LVDS pair can to 50 gbits/second within the range of projection.

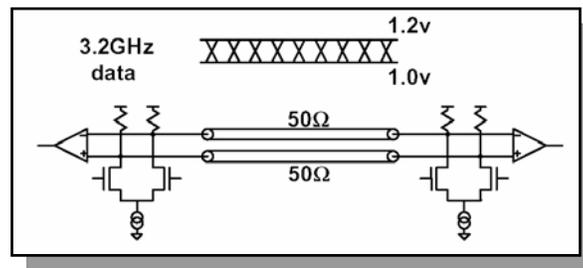


Figure 10: Low Voltage Differential Signaling

## No Obvious Winners

No obvious winner emerges from the graph. This is particularly notable because advocates of alternative architectures and packaging styles tout their approaches as being considerably more cost effective than existing systems.

## Conclusions

We believe our method has applicability beyond the analysis in this paper. In particular, the ITRS roadmap has adequate predictive power and supercomputer architectures are well enough understood that it is worth the effort to create a roadmap for supercomputer design. Predicting the future is notoriously difficult, as our experience with the change in the ITRS roadmap between 1999 and 2000 illustrated.

We successfully applied optimization techniques to supercomputer architecture. This could be useful in the future.

We conclude that LVDS has a fundamental advantage over pin-and-wire by using a software tool for "scenario analysis" of supercomputer architecture.

There was a widespread belief as recently as 1995, that a petaflop-level computer would be unachievable. This belief is not confirmed.

## Future Work

It should be possible to optimize supercomputer for actual applications rather than balance factors. With considerable analysis, one can model the runtime of some “computational kernels” on the abstract hardware like that produced by the planner<sup>[ref 4]</sup>. The optimizer could then find the architecture that offers the lowest cost per given speed of solution of some application. If this method could be applied to a weighted mix of applications, this would answer the question of “what machine is best for my applications.”

This form of analysis presupposes that computers will be built from the commercial chips covered by the ITRS. It does not account for wafer scale integration or non-CMOS devices. While CMOS technology has a huge maturity advantage over these other technologies, a subsequent analysis should cover them.

## References

1. Statement of Work for the Sandia Red Storm Computing Capability Development Program Procurement, RFQ Number 2999, Sandia National Laboratories
2. ASCI Purple RFP, Lawrence Livermore National Laboratory, <http://www.llnl.gov/ASCI/purple/>
3. 1999 and 2000 International Technology Roadmap for Semiconductors (ITRS), Semiconductor Industries Association (SIA) <http://public.itrs.net>
4. Predictive Performance and Scalability Modeling of a Large-Scale Application, Darren J. Kerbyson, Henry J. Alme, Adolfo Hoisie, Fabrizio Petrini, Harvey J. Wasserman, Michael L. Gittings, Proceedings of Supercomputing 2001.

## Appendix

### PIM Design Equations

Optimizer inputs: A node is an SMP with  $n$  CPU cores.

The chip area from the ITRS is allocated first to  $n$  CPU cores. The remaining chip area is divided by the memory density from the ITRS to get the amount of memory per PIM chip.

The signal pins are divided into 6 bundles, all for IPC IO.

DERATED FLOPS IS MINIMUM OF:	EXPLANATION:
$n \times \text{peak FLOPS per core}$	CPU FLOPS cannot exceed raw capability of CPU cores
$\frac{\text{ASIC I/O bandwidth}}{\text{IPC IO balance factor}}$	Derate CPU FLOPS as necessary to balance IPC IO bandwidth
$\frac{\text{memory capacity per core}}{\text{memory capacity balance factor}}$	Derate CPU FLOPS as necessary to balance memory size

Table 2: PIM Design Equations

Power computed by assuming the chip is  $x\%$  logic and  $(100-x)\%$  DRAM. The logic and DRAM scale from current levels by CMOS scaling rules.

### NCUBE Design Equations

Optimizer inputs: A node is an SMP with  $n$  CPU cores in the ASIC and  $m$  DRAM chips; the optimizer picks  $n$  and  $m$ .

The ASIC's signal pins are divided into 7 bundles: 6 of size  $x$  for IPC IO and one of size  $y$  for the memory bus.  $y = x \times \text{memory bandwidth balance factor} / \text{IPC IO balance factor}$ .

Derated Flops is minimum of:	Explanation:
$n \times \text{peak FLOPS per core}$	CPU FLOPS cannot exceed raw capability of CPU cores
$\frac{\text{router chip I/O bandwidth}}{\text{IPC IO balance factor}}$	Derate CPU FLOPS as necessary to balance IPC IO bandwidth
$\frac{m \times \text{memory capacity per DRAM}}{\text{memory capacity balance factor}}$	Derate CPU FLOPS as necessary to balance memory size
$\frac{\text{ASIC bus bandwidth}}{\text{memory bandwidth balance factor}}$	Derate CPU FLOPS as necessary to balance memory bus bandwidth at CPU
$\frac{m \times \text{memory bus bandwidth}}{\text{memory bandwidth balance factor}}$	Derate CPU FLOPS as necessary to balance memory bus bandwidth at memories

Table 3: nCUBE Design Equations

ASIC, DRAM and MPU cost from ITRS

### Discrete MPP Design Equations

Optimizer inputs: A node is an SMP with n CPU chips and m DRAM chips; the optimizer picks n and m.

Derated Flops is minimum of:	Explanation:
$n \times \text{peak FLOPS per CPU chip}$	CPU FLOPS cannot exceed raw capability of CPU cores
$\frac{\text{router chip I/O bandwidth}}{\text{IPC IO balance factor}}$	Derate CPU FLOPS as necessary to balance IPC IO bandwidth
$\frac{m \times \text{memory capacity per DRAM}}{\text{memory capacity balance factor}}$	Derate CPU FLOPS as necessary to balance memory size
$\frac{\text{CPU bus bandwidth}}{\text{memory bandwidth balance factor}}$	Derate CPU FLOPS as necessary to balance memory bus bandwidth at CPU
$\frac{m \times \text{memory bus bandwidth}}{\text{memory bandwidth balance factor}}$	Derate CPU FLOPS as necessary to balance memory bus bandwidth at memories

Table 4: Discrete MPP Design Equations

ASIC \$500, DRAM and MPU cost from ITRS

## Distribution:

1 MS	9037	J. C. Berry, 8945	1 MS	0818	P. Yarrington, 9230
1	9019	S. C. Carpenter, 8945	1	0819	R. M. Summers, 9231
1	9012	J. A. Friesen, 8963	1	0820	P. F. Chavez, 9232
1	9012	S. C. Gray, 8949	1	0316	S. S. Dosanjh, 9233
1	9011	B. V. Hess, 8941	1	0316	J. B. Aidun, 9235
1	9915	M. L. Koszykowski, 8961	1	0813	R. M. Cahoon, 9311
1	9019	B. A. Maxwell, 8945	1	0801	F. W. Mason, 9320
1	9012	P. E. Nielan, 8964	1	0806	C. Jones, 9322
1	9217	S. W. Thomas, 8962	1	0822	C. Pavlakos, 9326
1	0824	A. C. Ratzel, 9110	1	0807	J. P. Noe, 9328
1	0847	H. S. Morgan, 9120	1	0805	W.D. Swartz, 9329
1	0824	J. L. Moya, 9130	1	0812	M. R. Sjulín, 9330
1	0835	J. M. McGlaun, 9140	1	0813	A. Maese, 9333
1	0833	B. J. Hunter, 9103	1	0812	M. J. Benson, 9334
1	0834	M. R. Prarie, 9112	1	0809	G. E. Connor, 9335
1	0555	M. S. Garrett, 9122	1	0806	L. Stans, 9336
1	0821	L. A. Gritzo, 9132	1	1110	R. B. Brightwell, 9224
1	0835	E. A. Boucheron, 9141	1	1110	R. E. Riesen, 9223
1	0826	S. N. Kempka, 9113	1	1110	K. D. Underwood, 9223
1	0893	J. Pott, 9123	1	1110	E. P. DeBenedictis, 9223
1	1183	M. W. Pilch, 9133	1	0321	W. Camp, 9200
1	0835	K. F. Alvin, 9142	1	0841	T. Bickel, 9100
1	0834	J. E. Johannes, 9114	1	9003	K. Washington, 8900
1	0847	J. M. Redmond, 9124	1	0801	A. Hale, 9300
1	1135	S. R. Heffelfinger, 9134	1	0139	M. Vahle, 9900
1	0826	J. D. Zepper, 9143			
1	0825	B. Hassan, 9115			
1	0557	T. J. Baca, 9125	1	9018	Central Technical Files, 8945-1
1	0836	E. S. Hertel, Jr., 9116			
1	0847	R. A. May, 9126			
1	0836	R. O. Griffith, 9117	2	0899	Technical Library, 9616
1	0847	J. Jung, 9127			
1	0321	P. R. Graham, 9208			
1	0318	J. E. Nelson, 9209			
1	0847	S. A. Mitchell, 9211			
1	0310	M. D. Rintoul, 9212			
1	1110	D. E. Womble, 9214			
1	1111	B. A. Hendrickson, 9215			
1	0310	R. W. Leland, 9220			
1	1110	N. D. Pundit, 9223			
1	1110	D. W. Doerfler, 9224			
1	0847	T. D. Blacker, 9226			
1	0822	P. Heermann, 9227			

## Software

Note: the C++ software for the Petaflops Planner is included in the document bundle for the Sandia public release only. The actual software would be distributed separately and electronically.

```
// Planner.cpp : Defines the entry point for the console application.
//
#include "stdafx.h"

#include <stdio.h>
#include <math.h>
#include <string.h>

#if __GNUC__ != 0 // Linux
#include <sys/types.h>
#include <sys/stat.h>
#include <malloc.h>
#include <sys/socket.h>
#include <netinet/in.h>
#include <unistd.h>
#include <errno.h>
#define SOCKET int
#define INVALID_SOCKET -1
#define SOCKET_ERROR -1
int strcmp(const char *a, const char *b) { return strcmp(a, b); }
#define min(a, b) ((a) < (b) ? (a) : (b))
#define max(a, b) ((a) > (b) ? (a) : (b))
#else // Windows
#include <malloc.h>
#include <winsock.h>
#endif

#define ASSERT(c) if (!(c)) { fprintf(stderr, "assert failed"); fflush(stderr); char *p = NULL; *p++; }

#define BOOL int
#define FALSE 0

#define YEAR 2001

char *Index1 = "<font face=arial size=0>";
char *Index1a = "<font face=arial size=2>";
char *Index2 = "</font>";
char *Out1 = "<font face=arial size=0>";
char *Out1a = "<font face=arial size=2>";
char *Out1x = "";
char *Out1y = " bgcolor=yellow";
char *Out2 = "</font>";
char *Chip1 = "<font size=0 face=arial>";
char *Chip2 = "</font>";
char *DRAMColor1 = "#ffffc0";
char *DRAMColor2 = "#ffff80";
char *PCBColor = "#00ff00";
char *PCBoardGIF = "green.gif";
char *CPUCOLORA = "blue";
char *CPUCOLORB = "red";
char *navbkg = "#003366";
char *NOut1 = "<font face=arial size=0 color=white>";
char *NOut1a = "<font face=arial size=2 color=white>";
char *NOut1x = "";
char *NOut1y = " bgcolor=#319ace";
char *NOut2 = "</font>";
char *navlnk = "white";
char *navaln = "blue";
char *navvlnk = "pink";

int CS = 3;
int CP = 0;
#define SCALE 3.0

// speed of external wire compared to local clock
// .5 corresponds to dual-rail signalling at the local clock rate (full speed, but uses 2 pins per bit)
#define BUSFACTOR .5

char *GreekSuffix(double x) {
    static char dope[20]{1000};
    static int next = 0;
    static struct g {
        double limit;
        char *format;
        double divide;
    } table[] = {
        { 1e-11, "% .21fp", 1e-12, },
        { 1e-10, "% .11fp", 1e-12, },
        { 1e-9, "% .01fp", 1e-12, },
        { 1e-8, "% .21fn", 1e-9, },
        { 1e-7, "% .11fn", 1e-9, },
        { 1e-6, "% .01fn", 1e-9, },
        { 1e-5, "% .21fu", 1e-6, },
        { 1e-4, "% .11fu", 1e-6, },
        { 1e-3, "% .01fu", 1e-6, },
        { 1e-2, "% .21fm", 1e-3, },
        { 1e-1, "% .11fm", 1e-3, },
        { 1e0, "% .01fm", 1e-3, },
        { 1e1, "% .21f", 1, },
        { 1e2, "% .11f", 1, },
        { 1e3, "% .01f", 1, },
        { 1e4, "% .21fK", 1e3, },
        { 1e5, "% .11fK", 1e3, },
        { 1e6, "% .01fK", 1e3, },
        { 1e7, "% .21fM", 1e6, },
        { 1e8, "% .11fM", 1e6, },
        { 1e9, "% .01fM", 1e6, },
        { 1e10, "% .21fG", 1e9, },
        { 1e11, "% .11fG", 1e9, },
        { 1e12, "% .01fG", 1e9, },
        { 1e13, "% .21fT", 1e12, },
        { 1e14, "% .11fT", 1e12, },
    }
}
```

```

        { 1e15, "%.01fT", 1e12, },
        { 1e16, "%.21fP", 1e15, },
        { 1e17, "%.11fP", 1e15, },
        { 1e18, "%.01fP", 1e15, },
    };
    if (x == 0) {
        sprintf(dope[next%20], "0");
        return dope[next++%20];
    }
    for (unsigned int i = 0; i < sizeof(table)/sizeof(g); i++)
        if (x < table[i].limit) {
            sprintf(dope[next%20], table[i].format, x/table[i].divide);
            return dope[next++%20];
        }
    sprintf(dope[next%20], "%.01e", x);
    return dope[next++%20];
}

enum CoreType {
    RISC,
    VLIW,
    RED,
    NCUBE,
};

class Query {
public:
    double PerformanceTarget;
    CoreType Type;
    double IO_BytesPerSecondPerFlop1; // per link
    double IO_BytesPerSecondPerFlop2;
    double IO_BytesPerSecondPerFlopAll1; // all links together
    double IO_BytesPerSecondPerFlopAll2;
    double RAM_BytesPerFlop1; // memory size
    double RAM_BytesPerFlop2;
    double RAM_BytesPerSecondPerFlop1; // memory bandwidth
    double RAM_BytesPerSecondPerFlop2;
    double Realization1; // technology realization factor
    double Realization2;
    double Year;
    double Year1;
    double Year2;
    int class; // 0/1 -> 1 vs. 2 for balance factors
    int Units; // number of CPU cores or chips
    int Units1;
    int Units2;
    int Command;

    // convert a double, possibly with a GreekSuffix suffix
    void SD(double sd, char *v) {
        sscanf(v, "%lf", &sd);
        for (int i = strlen(v); --i >= 0; ) {
            if (v[i] == ' ') continue;
            else if (v[i] == 'f') d *= 1e-15;
            else if (v[i] == 'p') d *= 1e-12;
            else if (v[i] == 'n') d *= 1e-9;
            else if (v[i] == 'u') d *= 1e-6;
            else if (v[i] == 'm') d *= 1e-3;
            else if (v[i] == 'k' || v[i] == 'K') d *= 1e3;
            else if (v[i] == 'M') d *= 1e6;
            else if (v[i] == 'g' || v[i] == 'G') d *= 1e9;
            else if (v[i] == 't' || v[i] == 'T') d *= 1e12;
            else if (v[i] == 'P') d *= 1e15;
            else continue;
            break;
        }
    }

    // convert an integer, possibly with a GreekSuffix suffix
    void SI(int &n, char *v) {
        double d;
        sscanf(v, "%lf", &d);
        for (int i = strlen(v); --i >= 0; ) {
            if (v[i] == ' ') continue;
            else if (v[i] == 'f') d *= 1e-15;
            else if (v[i] == 'p') d *= 1e-12;
            else if (v[i] == 'n') d *= 1e-9;
            else if (v[i] == 'u') d *= 1e-6;
            else if (v[i] == 'm') d *= 1e-3;
            else if (v[i] == 'k' || v[i] == 'K') d *= 1e3;
            else if (v[i] == 'M') d *= 1e6;
            else if (v[i] == 'g' || v[i] == 'G') d *= 1e9;
            else if (v[i] == 't' || v[i] == 'T') d *= 1e12;
            else if (v[i] == 'P') d *= 1e15;
            else continue;
            break;
        }
        n = (int)d;
    }

    // construct a query, basing values on a previous submission
    Query(int argc, char **name, char **value) {
        PerformanceTarget = 1e15;
        Type = RISC;
        IO_BytesPerSecondPerFlop1 = 2; // per link
        IO_BytesPerSecondPerFlop2 = .1/12;
        IO_BytesPerSecondPerFlopAll1 = 2; // all links together
        IO_BytesPerSecondPerFlopAll2 = .1;
        RAM_BytesPerFlop1 = .5; // memory size
        RAM_BytesPerFlop2 = .5;
        RAM_BytesPerSecondPerFlop1 = 4; // memory bandwidth
        RAM_BytesPerSecondPerFlop2 = 4;
        Realization1 = 1; // technology realization factor
        Realization2 = 1;
        Year = 2010;

#if YEAR == 2000
        Year1 = 1999;
        Year2 = 2014;
#else
        Year1 = 2001;
        Year2 = 2016;
#endif

        Class = 0;
        Units = 6;
    }
};

```



```

        fprintf(out, "<tr><td>%sRealization factor</td><td>%s<input type=text size=8 name=r1 value=\"%s\">%s</td><td>%s<input
type=text size=8 name=r2 value=\"%s\">%s</td><td>%sfraction</td></tr>\n", Out1, Out2, Out1, GreekSuffix(Realization1), Out2, Out1,
GreekSuffix(Realization2), Out2, Out1, Out2);

        fprintf(out, "<tr><th>&nbsp;</th><th>%sFrom</th><th>%sTo</th><th>&nbsp;</th></tr>\n", Out1, Out2, Out1, Out2);
        fprintf(out, "<tr><td>%sPeriod</td><td>%s<input type=text size=8 name=y1 value=\"%d\">%s</td><td>%s<input type=text
size=8 name=y2 value=\"%d\">%s</td><td>%syear</td></tr>\n", Out1, Out2, Out1, (int)Year1, Out2, Out1, (int)Year2, Out2, Out1, Out2);
        fprintf(out, "<tr><td>%sUnits</td><td>%s<input type=text size=8 name=u1 value=\"%d\">%s</td><td>%s<input type=text
size=8 name=u2 value=\"%d\">%s</td><td>%sbytes/second/flop</td></tr>\n", Out1, Out2, Out1, Units1, Out2, Out1, Units2, Out2, Out1, Out2);
        fprintf(out, "<tr><td colspan=4 align=center><input type=submit name=cmd value=\"Calculate
Range\"></td></tr></table></td>\n");

        if (0) {

                fprintf(out, "<td valign=top><table border=1>\n");
                fprintf(out, "<tr><th>%sParameter</th><th>%sValue</th></tr>\n", Out1, Out2, Out1, Out2);
                fprintf(out, "<tr><td>%sClass:</td><td>%s<input type=radio name=class value=0>Data Intensive<br><input
type=radio name=class value=1>FLOPS Intensive</td></tr>\n",
                Out1, Out2, Out1,
                Class == 0 ? " checked" : "",
                Class != 0 ? " checked" : "",
                Out2);

                fprintf(out, "<tr><td>%sArchitecture:</td><td>%s<input type=radio name=arch value=RISC> RISC
PIM<br><input type=radio name=arch value=VLIW> VLIW PIM<br><input type=radio name=arch value=Red> Red<br><input type=radio name=arch
value=NCUBE> nCUBE</td></tr>\n",
                Out1, Out2, Out1,
                Type == RISC ? " checked" : "",
                Type == VLIW ? " checked" : "",
                Type == RED ? " checked" : "",
                Type == NCUBE ? " checked" : "",
                Out2);

                fprintf(out, "<tr><td>%sYear:</td><td>%s<input type=text size=8 name=y value=\"%d\">%s</td></tr>\n",
                Out1, Out2, Out1, (int)Year, Out2);
                fprintf(out, "<tr><td>%sUnits:</td><td>%s<input type=text size=8 name=u value=\"%d\">%s</td></tr>\n",
                Out1, Out2, Out1, Units, Out2);
                fprintf(out, "<tr><td colspan=2 align=center><input type=submit name=cmd
value=Display></td></tr></table></td>\n");
        }

        fprintf(out, "</tr></table></form>%s<br>\n", Out2);
};

struct Curve {
        double data[10];
        char *name;
        char *units;
} ITRS2001[10] = {
        {
                { { 2001, 2002, 2003, 2004, 2005, 2006, 2007, 2010, 2013, 2016, }, "year of production", },
                { { 130, 115, 100, 90, 80, 70, 65, 45, 32, 22, }, "DRAM 1/2 Pitch", "mm", },
                { { 150, 130, 107, 90, 80, 70, 65, 45, 32, 22, }, "MPU/ASIC 1/2 Pitch", "mm", },
                { { 90, 75, 65, 53, 45, 40, 35, 25, 18, 13, }, "MPU Printed Gate Length", "nm", },
                { { 65, 53, 45, 37, 32, 28, 25, 18, 13, 9, }, "MPU Physical Gate Length", "nm", },
        },
        {
                { { 0, }, "", },
        },
        {
                { { 0, }, "", },
        },
        {
                { { 0, }, "", },
        },
        {
                { { 1684, 2317, 3088, 3990, 5173, 5631, 6739, 11511, 19348, 28751, }, "On-chip Local Clock", "MHz", },
                { { 1684, 2317, 3088, 3990, 5173, 5631, 6739, 11511, 19348, 28751, }, "Chip-to-board (off-chip) speed", "MHz", },
        },
        {
                { { 0, }, "", },
        },
        {
                { { 1.1, 1.0, 1.0, 1, .9, .9, 7, .6, .5, .4, }, "Vdd (high performance)", "v", },
        },
};

class RoadmapBase {
public:
        double Year;

        double Interpolate(double *vec) {
#if YEAR == 2000
                static double RoadmapYears[10] = { 1999, 2000, 2001, 2002, 2003, 2004, 2005, 2008, 2011, 2014, };
#else
                static double RoadmapYears[10] = { 2001, 2002, 2003, 2004, 2005, 2006, 2007, 2010, 2013, 2016, };
#endif
                if (Year <= RoadmapYears[0]) return vec[0];

                for (int i = 0; i < 9; i++)
                        if (Year >= RoadmapYears[i] && Year < RoadmapYears[i+1]) {
                                double frac = (Year - RoadmapYears[i]) / (RoadmapYears[i+1] - RoadmapYears[i]);
                                return vec[i] * (1.0 - frac) + vec[i+1] * frac;
                        }
                return vec[9];
        }

        double I(Curve *c, double Y) {
                if (Y <= Dat(0, 0, 0)) return c->data[0];

                for (int i = 0; i < 9; i++)
                        if (Y >= Dat(0, 0, i) && Y < Dat(0, 0, i+1)) {
                                double frac = (Y - Dat(0, 0, i)) / (Dat(0, 0, i+1) - Dat(0, 0, i));
                                return c->data[i] * (1.0 - frac) + c->data[i+1] * frac;
                        }
                return c->data[9];
        }

        Curve *D(int Table, int Index) {
                return &ITRS2001[Table][Index];
        }
};

```

```

Curve *DByName(char *key) {
    for (int i = 0; i < 10; i++)
        for (int j = 0; j < 10; j++) {
            Curve *t = &ITRS2001[i][j];
            if (t->name == NULL) break;
            if (strstr(t->name, key) != NULL)
                return t;
        }
    return NULL;
}

double Dat(int Table, int Index, int Time) {
    return D(Table, Index)->data[Time];
}

/*
double ITRSAtYear(int Table, int Index, double Y) {
    if (Y <= Dat(0, 0, 0)) return Dat(Table, Index, 0);

    for (int i = 0; i < 9; i++)
        if (Y >= Dat(0, 0, i) && Y < Dat(0, 0, i+1)) {
            double frac = (Y-Dat(0, 0, i)) / (Dat(0, 0, i+1)-Dat(0, 0, i));
            return Dat(Table, Index, i) * (1.0-frac) + Dat(Table, Index, i+1) * frac;
        }
}
*/

double ITRS(char *key, double Y) {
    Curve *c = DByName(key);
    if (c == NULL) return 0.0;
    return I(c, Y);
}

double ITRS(char *key) {
    return ITRS(key, Year);
}

};

class Technology: public RoadmapBase {
public:
    virtual double MaxFunctionsPerChip() = 0; // transistors (logic) or bits (DRAM)
    virtual double MaxChipSize() = 0; // square millimeters
    virtual double LocalClock() = 0; // intra-chip clock
    virtual double ChipToBoardFast() = 0; // speed to PC board
    virtual double Pads() = 0; // I/O pads
    virtual double HighPerformanceCoreSize() { return 0.0; }
    virtual double GBitsCm() = 0; // if memory -> gigabits per square centimeter
    virtual double CellArea() = 0; // if memory -> square microns per bit
    virtual double Cost() = 0; // cost per functional unit
    virtual char *Name() = 0;
};

class ASIC_Class: public Technology {
public:
    double MaxFunctionsPerChip() { // million transistors
#ife YEAR == 2000
        static double data[10] = { 157, 223, 315, 426, 411, 556, 751, 1852, 4568, 11269, };
#efse
        static double data[10] = { 714, 899, 810, 1020, 1286, 1620, 2041, 4081, 8163, 16326, }; // 2002 1i & 1j
#endif
        return Interpolate(data);
    }

    double MaxChipSize() { // square millimeters
#define DIESQMM 1600
#define ASICCOST 2000
#ife YEAR == 2000
        static double data[10] = { 800, 800, 800, 800, 572, 572, 572, 572, 572, 572, };
#efse
        static double data[10] = { DIESQMM, DIESQMM, DIESQMM, DIESQMM, DIESQMM, DIESQMM, DIESQMM, DIESQMM, DIESQMM, DIESQMM, };
// 2002 1i & 1j
#endif
        return Interpolate(data);
    }

    double LocalClock() { // megahertz
#ife YEAR == 2000
        static double data[10] = { 1250, 1620, 2100, 2490, 2952, 3500, 4150, 7115, 11050, 14920, };
#efse
        static double data[10] = { 1684, 2317, 3088, 3990, 5173, 5631, 6739, 11511, 19348, 28751, }; // 2002 4c & 4d
#endif
        return Interpolate(data);
    }

    double ChipToBoardFast() { // megahertz
#ife YEAR == 2000
        static double data[10] = { 1200, 1386, 1600, 1724, 1857, 2000, 2155, 2655, 3190, 3825, };
#efse
        static double data[10] = { 1684, 2317, 3088, 3990, 5173, 5631, 6739, 11511, 19348, 28751, }; // 2002 4c & 4d
#endif
        return Interpolate(data);
    }

    double Pads() { // pads
#ife YEAR == 2000
        static double data[10] = { 700, 900, 1100, 1300, 1500, 1700, 1900, 2300, 2700, 3000, };
#efse
        static double data[10] = { 1500, 1600, 1700, 1800, 2000, 2100, 2200, 2400, 2700, 3000, }; // 2002 3a & 3b
#endif
        return Interpolate(data);
    }

    double GBitsCm() { return 0.0; }
    double CellArea() { return 0.0; }
    // No referencable data
    // $1000.00 per ASIC
    double Cost() { // packaged microcents per transistor
        return ASICCOST * 100. / MaxFunctionsPerChip();
    }

    char *Name() { return "ASIC"; }
};

class HighPerformanceMPU_Class: public Technology {
public:
    double MaxFunctionsPerChip() { // million transistors
#ife YEAR == 2000

```

```

static double data[10] = { 61, 86, 122, 173, 244, 345, 488, 1381, 3907, 11052, };
#else
static double data[10] = { 276, 348, 439, 553, 697, 878, 1106, 2212, 4424, 8848, }; // 2002 1i & 1j
#endif
return Interpolate(data);
}

double MaxChipSize() { // million transistors
#if YEAR == 2000
static double data[10] = { 310, 310, 310, 325, 340, 356, 372, 427, 489, 561, };
#else
static double data[10] = { 310, 310, 310, 310, 310, 310, 310, 310, 310, 310, }; // 2002 1i & 1j
#endif
return Interpolate(data);
}

double LocalClock() { // megahertz
#if YEAR == 2000
static double data[10] = { 1250, 1620, 2100, 2490, 2952, 3500, 4150, 7115, 11050, 14920, };
#else
static double data[10] = { 1684, 2317, 3088, 3990, 5173, 5631, 6739, 11511, 19348, 28751, }; // 2002 4c & 4d
#endif
return Interpolate(data);
}

double ChipToBoardFast() { // megahertz
#if YEAR == 2000
static double data[10] = { 1200, 1386, 1600, 1724, 1857, 2000, 2155, 2655, 3190, 3825, };
#else
static double data[10] = { 1684, 2317, 3088, 3990, 5173, 5631, 6739, 11511, 19348, 28751, }; // 2002 4c & 4d
#endif
return Interpolate(data);
}

// WRONG!!
double Pads() { // pads
#if YEAR == 2000
static double data[10] = { 700, 900, 1100, 1300, 1500, 1700, 1900, 2300, 2700, 3000, };
#else
static double data[10] = { 1500, 1600, 1700, 1800, 2000, 2100, 2200, 2400, 2700, 3000, }; // 2002 3a & 3b
#endif
return Interpolate(data);
}

double HighPerformanceCoreSize() { // million transistors
#if YEAR == 2000
static double data[10] = { 12, 17, 24, 33, 47, 65, 94, 265, 700, 2100, }; // derived from Kahng 18 July 2001
"work in progress" with Erik's adjustments from HighPerformanceMPUFunctionsPerChip
#else
static double data[10] = { 24, 33, 47, 65, 100, 150, 200, 600, 1500, 3200, }; // (extended by Erik) derived from
Kahng 18 July 2001 "work in progress" with Erik's adjustments from HighPerformanceMPUFunctionsPerChip
#endif
return Interpolate(data);
}

double GBitsCm() { return 0.0; }
double CellArea() { return 0.0; }
double Cost() { // packaged microcents per transistor
#if YEAR == 2000
static double data[10] = { 245, 174/**/, 123, 86/**/, 61, 43/**/, 31, 11/**/, 3.8, 1.35/**/, };
#else
static double data[10] = { 97, 69, 49, 34, 24, 17, 12, 4.31, 1.52, .54, }; // 2002 7a & 7b
#endif
return Interpolate(data);
}

char *Name() { return "High Performance MPU"; }
};

class DRAMProductionClass: public Technology {
public:
double MaxFunctionsPerChip() { return MaxChipSize() / CellArea(); }
double MaxChipSize() { // square millimeters
#if YEAR == 2000
static double data[10] = { 131, 129, 127, 141, 157, 175, 147, 205, 191, 268, };
#else
static double data[10] = { 127, 100, 118, 93, 147, 116, 183, 181, 239, 238, }; // 2002 1c & 1d
#endif
return Interpolate(data);
}

double LocalClock() { return 0.0; }
double ChipToBoardFast() { return 0.0; }
double Pads() { return 256; }

double GBitsCm() { // gigabits/square centimeter
#if YEAR == 2000
static double data[10] = { .2, .29, .42, .54, .68, .87, 1.46, 2.97, 8.99, 18.1, };
#else
static double data[10] = { .42, .54, .91, 1.15, 1.46, 1.85, 2.35, 4.75, 14.25, 28.85, }; // 2002 1c & 1d
#endif
return Interpolate(data);
}

double CellArea() { // square microns
#if YEAR == 2000
static double data[10] = { .26, .18, .13, .1, .082, .065, .039, .019, .0064, .0032, };
#else
static double data[10] = { .13, .103, .061, .049, .039, .031, .024, .012, .004, .002, }; // 2002 1c & 1d
#endif
return Interpolate(data);
}

double Cost() { // packaged microcents per bit
#if YEAR == 2000
static double data[10] = { 15, 10.5/**/, 7.6, 5.3/**/, 3.8, 2.6/**/, 1.9, .675/**/, .24, .085/**/, };
#else
static double data[10] = { 7.7, 5.4, 3.8, 2.7, 1.9, 1.4, .96, .34, .12, .042, }; // 2002 7a & 7b
#endif
return Interpolate(data);
}

char *Name() { return "DRAM Production"; }
};

class DRAMIntroductionClass: public Technology {
public:
double MaxFunctionsPerChip() { return MaxChipSize() / CellArea(); }
double MaxChipSize() { // square millimeters
#if YEAR == 2000
static double data[10] = { 400, 395, 390, 435, 485, 542, 454, 516, 392, 448, };
#else
static double data[10] = { 390, 308, 364, 287, 454, 359, 568, 563, 373, 186, }; // 2002 1e & 1f
#endif
return Interpolate(data);
}
};

```

```

        return Interpolate(data);
    }
    double LocalClock() { return 0.0; }
    double ChipToBoardFast() { return 0.0; }
    double Pads() { return 128; }

    double GBitsCm() { // gigabits/square centimeter
    #if YEAR == 2000
        static double data[10] = { .27, .38, .55, .70, .88, 1.12, 1.89, 3.82, 11.56, 23.25, };
    #else
        static double data[10] = { .55, .7, 1.18, 1.49, 1.89, 2.39, 3.03, 6.1, 18.42, 37.1, }; // 2002 1e & 1f
    #endif
        return Interpolate(data);
    }
    double CellArea() { // square microns
    #if YEAR == 2000
        static double data[10] = { .26, .18, .13, .1, .082, .065, .039, .019, .0064, .0032, };
    #else
        static double data[10] = { .13, .103, .061, .049, .039, .031, .024, .012, .004, .002, }; // 2002 1e & 1f
    #endif
        return Interpolate(data);
    }
    double Cost() { // packaged microcents per bit
    #if YEAR == 2000
        static double data[10] = { 42, 30/**/, 21, 15/**/, 11, 7.5/**/, 5.3, 1.8/**/, .66, .23/**/, };
    #else
        static double data[10] = { 21, 14.8, 10.5, 7.4, 5.3, 3.7, 2.6, .93, .33, .12, }; // 2002 1e & 1f
    #endif
        return Interpolate(data);
    }
    char *Name() { return "DRAM Introduction"; }
};

// implement the SIA Roadmap for Semiconductors
class Roadmap: public RoadmapBase {
public:
    ASIC_Class ASIC;
    HighPerformanceMPU_Class HighPerformanceMPU;
    DRAMIntroductionClass DRAMIntroduction;
    DRAMProductionClass DRAMProduction;

    Roadmap(double y) {
        Year = y;
        ASIC.Year = y;
        HighPerformanceMPU.Year = y;
        DRAMIntroduction.Year = y;
        DRAMProduction.Year = y;
    }

    #if 0
    double DRAMHalfPitch() { // nanometers
        static double dataDRAMHalfPitch[10] = { 180, 150, 130, 115, 100, 90, 80, 60, 40, 30, };
        return Interpolate(dataDRAMHalfPitch);
    }
    double Roadmap::DRAMCellArea() { // square microns
        static double dataDRAMCellArea[10] = { .26, .18, .13, .1, .082, .065, .039, .019, .0064, .0032, };
        return Interpolate(dataDRAMCellArea);
    }
    double HighPerformanceMPUCoreSize() { // million transistors
        static double dataHighPerformanceMPUCoreSize[10] = { 12, 17, 24, 33, 47, 65, 94, 265, 700, 2100, }; // derived
        return Interpolate(dataHighPerformanceMPUCoreSize);
    }

    double Roadmap::LocalClockAcrossChip() { // megahertz
        static double dataLocalClock[10] = { 1200, 1386, 1600, 1724, 1857, 2000, 2155, 2655, 3190, 3825, };
        return Interpolate(dataLocalClock);
    }

    double Roadmap::ASICClock() { // megahertz
        static double dataASICClock[10] = { 500, 559, 626, 700, 761, 828, 900, 1200, 1500, 1800, };
        return Interpolate(dataASICClock);
    }

    double Roadmap::ChipToBoard() { // megahertz
        static double dataChipToBoard[10] = { 480, 589, 722, 885, 932, 982, 1035, 1285, 1540, 1800, };
        return Interpolate(dataChipToBoard);
    }

    #endif
};

class Chip {
public:
    Technology *Tech;

    char *Name;
    int Number;

    double SqMM;

    int CPUCores;
    double FLOPS;
    double CLKMHZ;

    double BytesDRAM;

    int IOPads3d;
    double IOBandwidth3d;

    int MemPads;
    double BusBandwidth;

    double CostPerChip;

    Chip();
    void SetTech(Technology *t) { Tech = t; SqMM = Tech->MaxChipSize(); CostPerChip = Tech->MaxFunctionsPerChip() * Tech->Cost() /
100.; }
    //
    double HighPerformanceCoreSize() { return Tech != NULL ? Tech->HighPerformanceCoreSize() : 0.0; }
    double Power() {
        double S = Tech->ITRS("MPU/ASIC 1/2 Pitch") / Tech->ITRS("MPU/ASIC 1/2 Pitch", 1990);
        double Vdd = Tech->ITRS("Vdd (high performance)");
        double CLKRatio = Tech->ITRS("On-chip Local Clock") / Tech->ITRS("On-chip Local Clock", 1990);
        double Pwr = S * Vdd * Vdd / Tech->ITRS("Vdd (high performance)", 1990) / Tech->ITRS("Vdd (high performance)", 1990);
        double Pwr200X;
    }
};

```

```

        double BaseCPU = 100, BaseMem = 1, BaseRouter = 2;
        if (CPUCores > 0 && BytesDRAM > 0) {
            Pwr200X = BaseMem * Pwr * ClkRatio / S / S;
            Pwr200X = CPUCores * BaseCPU * Pwr * ClkRatio;
        }
        else if (CPUCores > 0)
            Pwr200X = BaseCPU * Pwr * ClkRatio / S / S;
        else if (BytesDRAM > 0)
            Pwr200X = BaseMem * Pwr * ClkRatio / S / S;
        else
            Pwr200X = BaseRouter * Pwr * ClkRatio / S / S;
        return Pwr200X;
    }
    void Print(FILE *);
};

Chip::Chip() {
    Tech = NULL;
    Name = NULL;
    Number = 0;

    SqMM = 0.0;

    CPUCores = 0;
    FLOPS = 0.0;
    ClkMHz = 0.0;

    BytesDRAM = 0.0;

    IOPads3d = 0;
    IOBandwidth3d = 0.0;

    MemPads = 0;
    BusBandwidth = 0.0;
}

void Chip::Print(FILE *out) {
    if (Number == 0) return;
    fprintf(out, "<h2>%s</h2>\n", Name);
    fprintf(out, "Implemented with %s technology<br>\n", Tech->Name());

    double S = Tech->ITRS("MPU/ASIC 1/2 Pitch") / Tech->ITRS("MPU/ASIC 1/2 Pitch", 1990);
    double Vdd = Tech->ITRS("Vdd (high performance)");
    double ClkRatio = Tech->ITRS("On-chip Local Clock") / Tech->ITRS("On-chip Local Clock", 1990);
    double Pwr = S * Vdd * Vdd / Tech->ITRS("Vdd (high performance)", 1990) / Tech->ITRS("Vdd (high performance)", 1990);

    double Pwr200X;
    double BaseCPU = 100, BaseMem = 1, BaseRouter = 2;
    if (CPUCores > 0 && BytesDRAM > 0) {
        Pwr200X = BaseMem * Pwr * ClkRatio / S / S;
        Pwr200X = CPUCores * BaseCPU * Pwr * ClkRatio;
    }
    else if (CPUCores > 0)
        Pwr200X = BaseCPU * Pwr * ClkRatio / S / S;
    else if (BytesDRAM > 0)
        Pwr200X = BaseMem * Pwr * ClkRatio / S / S;
    else
        Pwr200X = BaseRouter * Pwr * ClkRatio / S / S;

    fprintf(out, "1/2 pitch %.01f->%.01f S-%.21f\n", Tech->ITRS("MPU/ASIC 1/2 Pitch", 1990), Tech->ITRS("MPU/ASIC 1/2 Pitch", S),
    fprintf(out, "Vdd = %.21f ClkRatio = %.01f Power=%s fixed %s grow<br>\n", Vdd, ClkRatio, GreekSuffix(Pwr * ClkRatio),
    GreekSuffix(Pwr * ClkRatio / S / S));
    fprintf(out, "%s<br>\n", GreekSuffix(Pwr200X));

    if (Number == 1) fprintf(out, "%%.21f<br>\n", CostPerChip);
    else fprintf(out, "%%.21f (%d repetitions of this chip @ %%.21f)<br>\n", CostPerChip * Number, Number, CostPerChip);

    if (SqMM != 0.0) fprintf(out, "%%.11f Sq MM<br>\n", SqMM);

    if (CPUCores != 0) fprintf(out, "%d CPU Cores<br>\n", CPUCores);
    if (FLOPS > 1e8) fprintf(out, "%%.11f GFLOPS<br>\n", FLOPS/1e9);
    else if (FLOPS != 0.0) fprintf(out, "%%.11f MFLOPS<br>\n", FLOPS/1e6);

    if (ClkMHz > 1e2) fprintf(out, "%%.11f GHz Clock<br>\n", ClkMHz/1e3);
    else if (ClkMHz != 0.0) fprintf(out, "%%.11f MHz Clock<br>\n", ClkMHz);

    if (BytesDRAM * Number > 2e9) fprintf(out, "%%.11f GBytes DRAM (%d repetitions of chip with %%.11f Mbits)<br>\n", Number *
    BytesDRAM/1024./1024., Number, BytesDRAM/1024./1024.*8);
    else if (BytesDRAM != 0.0) fprintf(out, "%%.11f MBytes DRAM (%d repetitions of chip with %%.11f Mbits)<br>\n", Number *
    BytesDRAM/1024./1024., Number, BytesDRAM/1024./1024.*8);

    if (IOBandwidth3d != 0) fprintf(out, "%sBytes/s x 6 I/O bandwidth on %d x 6 pins<br>\n", GreekSuffix(IOBandwidth3d), IOPads3d);

    if (BusBandwidth != 0) fprintf(out, "%sBytes/s bus bandwidth on %d pins<br>\n", GreekSuffix(BusBandwidth), MemPads);

    double PinScale = .075;

    int TotalPins = (int)(Tech->Pads() * PinScale);
    int BusPins = (int)(MemPads * PinScale);
    if (BusPins == 0) BusPins++;
    int IOPins = (int)(IOPads3d * PinScale);
    int UnusedPins = TotalPins - BusPins - 6*IOPins;

    fprintf(out, "<table border=1 cellspacing=0 cellpadding=0 align=center><tr><th>%s</th></tr><tr><td>\n", Index1,
    (int)Tech->Pads(), Index2);
    fprintf(out, "<table border=0 cellspacing=0 cellpadding=0>\n");
    for (int i = 0, e = Number > 1 ? Number : 1; i < e; i++) {
        if (i != 0)
            fprintf(out, "<tr></tr>\n");
        fprintf(out, "<tr>\n");
        if (IOPins > 0)
            for (int j = 0; j < 6; j++)
                fprintf(out, "<td><img src=%s.gif width=%d height=10></td>\n", j%2 ? "blue" : "red", IOPins);
        fprintf(out, "<td><img src=yellow.gif width=%d height=10></td>\n", BusPins);
        if (UnusedPins > 0)
            fprintf(out, "<td><img src=green.gif width=%d height=10></td>\n", UnusedPins);
        fprintf(out, "</tr>");
    }
    fprintf(out, "</table>\n");
    fprintf(out, "</td></tr>");
    fprintf(out, "<tr><td>%sRed/Blue = I/O Link<br>Yellow = Memory Bus<br>Green = Available<td></tr>\n", Index1, Index2);
    fprintf(out, "</table>\n");
}

```



```

        if (i) for (int i = 0; i < RAMArray; i++) {
            fprintf(out, "<tr>\n");
            for (int j = 0; j < RAMArray; j++)
                if ((RAMArray-1-l)*RAMArray + j < RamChips)
                    fprintf(out, "<td><img src=%s height=%d width=1></td>"
                            "<td bgcolor=%s align=center>%sDRAM%s</td>"
                            "<td><img src=%s height=%d width=1></td>\n", PCBoardGIF, DRAMEdge,
                            (i+j)%2 ? DRAMColor1 : DRAMColor2, Chip1, Chip2, PCBoardGIF, DRAMEdge);
            fprintf(out, "<tr>\n");
        }
        fprintf(out, "</table>\n"); // c

        fprintf(out, "</td></tr><tr><td valign=top>\n"); // a/b c

        int RouterEdge = (int)(SCALE * sqrt(CPUSz));
        fprintf(out, "<table border=0 cellspacing=0 cellpadding=0 align=left>\n"); // b
        fprintf(out, "<tr><td><img src=%s width=1 height=1></td><td><img src=%s width=%d height=1></td><td><img src=%s width=1
height=1></td></tr>\n", PCBoardGIF, PCBoardGIF, RouterEdge, PCBoardGIF);
        fprintf(out, "<tr><td><img src=%s width=1 height=%d></td><td align=center bgcolor=black><font
color=white>%s</font></td><td><img src=%s width=1 height=%d></td></tr>\n", PCBoardGIF, RouterEdge, Chip1, "Router", Chip2, PCBoardGIF,
RouterEdge);
        fprintf(out, "<tr><td><img src=%s width=1 height=1></td><td><img src=%s width=%d height=1></td><td><img src=%s width=1
height=1></td></tr>\n", PCBoardGIF, PCBoardGIF, RouterEdge, PCBoardGIF);
        fprintf(out, "</table>\n"); // b

        fprintf(out, "</td></tr></table>\n"); // a/b c
        fprintf(out, "</td></tr></table>\n"); // border
    }

// output HTML for a PIM type chip
class PIMPicture: public Picture {
public:
    void Print();
};

void PIMPicture::Print() {
    int Units = CPUChips;

    double ChipEdge = sqrt(CPUSz + DRAMSz);
    double CPUEdge = sqrt(CPUSz);
    // double Border = (ChipEdge-CPUEdge)/2;

    int iPad = 2;

    // char *fontsize="size=-12 color=green";

    double scale = SCALE;
    int iEdge = (int)(scale*ChipEdge);
    int iCPUEdge = (int)(scale*CPUEdge);
    int iBorder = (iEdge - iCPUEdge)/2;
    if (iBorder + iBorder + iCPUEdge < iEdge) iCPUEdge++;

    if (out == NULL)
        return;

    // cut number of units to prevent CPUs less than one pixel
    if (Units > iCPUEdge)
        Units = iCPUEdge;

    // 1-pixel top line to control spacing
    fprintf(out, "<table border=0 cellspacing=0 cellpadding=0 align=center>\n"
            "<tr><td><img src=black.gif width=%d height=%d></td>\n"
            "<td><img src=black.gif width=%d height=%d></td>\n", iPad, iPad, iBorder, iPad);
    if (i) for (int i = 0; i < Units; i++) {
        int left = i * iCPUEdge / Units;
        int right = (i+1) * iCPUEdge / Units;
        fprintf(out, "<td><img src=black.gif width=%d height=%d></td>\n", right-left, iPad);
    }
    fprintf(out, "<td><img src=black.gif width=%d height=%d></td>\n"
            "<td><img src=black.gif width=%d height=%d></td></tr>\n\n", iBorder, iPad, iPad, iPad);

    // top DRAM region
    char note[100];
    sprintf(note, Units == 1 ? "CPU" : "%d PIM CPUs", Units);
    fprintf(out, "<tr><td><img src=black.gif width=%d height=%d></td>\n"
            "<td colspan=%d valign=bottom><img src=yellow.gif width=%d height=%d></td>\n"
            "<td><img src=black.gif width=%d height=%d></td></tr>\n\n", iPad, iBorder, Units+2, iEdge, iBorder, iPad,
iBorder);

    // center DRAM-CPU-DRAM region
    fprintf(out, "<tr><td><img src=black.gif width=%d height=%d></td>\n"
            "&td><img src=yellow.gif width=%d height=%d></td>\n", iPad, iCPUEdge, iBorder, iCPUEdge);
    if (i) for (int i = 0; i < Units; i++) {
        int left = i * iCPUEdge / Units;
        int right = (i+1) * iCPUEdge / Units;
        fprintf(out, "<td><img src=%s width=%d height=%d></td>\n", (i%2) ? "red.gif" : "blue.gif", right-left, iCPUEdge);
    }
    fprintf(out, "<td><img src=yellow.gif width=%d height=%d></td>\n"
            "&td><img src=black.gif width=%d height=%d></td></tr>\n\n", iBorder, iCPUEdge, iPad, iCPUEdge);

    // bottom DRAM region (with CPU legend)
    fprintf(out, "<tr><td><img src=black.gif width=%d height=%d></td>\n"
            "&td colspan=%d><img src=yellow.gif width=%d height=%d></td>\n"
            "&td><img src=black.gif width=%d height=%d></td></tr>\n\n", iPad, iBorder, 2+Units, iEdge, iBorder, iPad,
iBorder);

    // 1-pixel bottom line to set spacing
    fprintf(out, "<tr><td><img src=black.gif width=%d height=%d></td>\n"
            "&td><img src=black.gif width=%d height=%d></td>\n", iPad, iPad, iBorder, iPad);
    if (i) for (int i = 0; i < Units; i++) {
        int left = i * iCPUEdge / Units;
        int right = (i+1) * iCPUEdge / Units;
        fprintf(out, "<td><img src=black.gif width=%d height=%d></td>\n", right-left, iPad);
    }
    fprintf(out, "<td><img src=black.gif width=%d height=%d></td>\n"
            "&td><img src=black.gif width=%d height=%d></td></tr>\n</table>\n\n", iBorder, iPad, iPad, iPad);

    return;
}

```

```

void GIFHeader(SOCKET theClient) {
    send(theClient, "HTTP/1.0 200\r\n", 14, 0);
    send(theClient, "Content-type: ", 14, 0);
    send(theClient, "image/gif", 9, 0);
    send(theClient, "\r\n", 2, 0);
    send(theClient, "\r\n", 2, 0);
}

// helper to write a 1x1 pixel gif of a certain color
void SmallGIFHelper(SOCKET theClient, unsigned char *tail) {
    GIFHeader(theClient);
    unsigned char header[73] = { 71, 73, 70, 56, 55, 97, 1, 0, 1, 0, 179, 0, 0, 0, 0, 128, 0, 0, 0, 128, 0, 128, 128, 0, 0, 0, 128,
    128, 0, 128, 0, 128, 192, 192, 192, 128, 128, 128, 255, 0, 0, 0, 255, 0, 255, 255, 0, 0, 0, 255, 255, 0, 255, 255, 255, 255, 255,
    44, 0, 0, 0, 0, 1, 0, 1, 0, 0, 4, 2, };
    send(theClient, (char *)header, 73, 0);
    send(theClient, (char *)tail, 4, 0);
}

// helper to write a 1x1 pixel gif of a certain color
void BigGIFHelper(SOCKET theClient, unsigned char *data, int len) {
    GIFHeader(theClient);
    send(theClient, (char *)data, len, 0);
}

// Plan an MPP in accordance with the query
// return value indicates an impossible design (error)
// return price per node and units per designated overall performance
int FloorPlanner(FILE *out, Query &qx, double &DollarsPerNode, double &UnitsPerPetaFlop) {
    int rval = 0; // error

    double IO_BytesPerSecondPerFlop = qx.Class == 0 ? qx.IO_BytesPerSecondPerFlop1 : qx.IO_BytesPerSecondPerFlop2; // per link
    double IO_BytesPerSecondPerFlopAll = qx.Class == 0 ? qx.IO_BytesPerSecondPerFlopAll1 : qx.IO_BytesPerSecondPerFlopAll2; // all
links together
    double RAM_BytesPerFlop = qx.Class == 0 ? qx.RAM_BytesPerFlop1 : qx.RAM_BytesPerFlop2; // memory
size
    double RAM_BytesPerSecondPerFlop = qx.Class == 0 ? qx.RAM_BytesPerSecondPerFlop1 : qx.RAM_BytesPerSecondPerFlop2; // memory
bandwidth
    double Realization = qx.Class == 0 ? qx.Realization1 : qx.Realization2;

    double MemoryDerator = pow(qx.PerformanceTarget/20e12, -.25);
    RAM_BytesPerFlop *= MemoryDerator;

    Roadmap y(qx.Year);

    // draw navigation portion
    if (out != NULL) {
        fprintf(out, "<html><head><title>%d %s for %d</title></head>\n", qx.Units,
        qx.Type == RISC ? "RISC CPU PIM" : qx.Type == VLIW ? "VLIW CPU PIM" : qx.Type == RED ? "CPU Red MPP" : "CPU
Core nCUBE/Blue Light",
        (int)qx.Year);
        fprintf(out, "<body background='bkgrnd.gif' text='#000000' link='#003366' vlink='#cc0033' alink='#000000'>\n");
        fprintf(out, "<a name='TOP'></a>\n");
        fprintf(out, "<table border='0' width='100%'>\n");
        fprintf(out, "<tr valign='top'><td>\n");
        fprintf(out, "<table border='0' width='140' valign='top'>\n");
        fprintf(out, "<tr valign='top'><td width='140' valign='top'>\n");
        fprintf(out, "\n");
        //
        fprintf(out, "<font color=white>Nav text</font>");

        fprintf(out, "<table align=center cellpadding=0 cellspacing=0><tr><td><table>\n");
        fprintf(out, "<tr><td></td><td align=center colspan=2><a href=/index.htm target=query>%sIndex</a><br><a
href=/help.htm>%sHelp</a></td><td></td></tr>\n", NOut1, NOut2, NOut1, NOut2);

        // navigate years
        if (qx.Year == qx.Year1)
            fprintf(out, "<tr><td align=center>%s</td>", NOut1, NOut2);
        else {
            qx.Year--;
            fprintf(out, "<tr><td align=center><a href=%s>%s</a></td>", qx.OutURL(), NOut1, ((int)qx.Year), NOut2);
            qx.Year++;
        }
        fprintf(out, "<td align=center colspan=2>%s</td>", NOut1, NOut1, (int)qx.Year, NOut2);
        if (qx.Year == qx.Year2)
            fprintf(out, "<td align=center>%s</td></tr>\n", NOut1, NOut2);
        else {
            qx.Year++;
            fprintf(out, "<td align=center><a href=%s>%s</a></td></tr>\n", qx.OutURL(), NOut1, (int)qx.Year,
            NOut2);
            qx.Year--;
        }

        // navigate units
        if (qx.Units == qx.Units1)
            fprintf(out, "<tr><td align=center>%s</td>", NOut1, NOut2);
        else {
            qx.Units--;
            fprintf(out, "<tr><td align=center><a href=%s>%s<br>CPUs</a></td>", qx.OutURL(), NOut1, qx.Units,
            NOut2);
            qx.Units++;
        }
        fprintf(out, "<td align=center colspan=2>%s<br>CPUs</td>", NOut1, NOut1, qx.Units, NOut2);
        if (qx.Units == qx.Units2)
            fprintf(out, "<td align=center>%s</td></tr>\n", NOut1, NOut2);
        else {
            qx.Units++;
            fprintf(out, "<td align=center><a href=%s>%s<br>CPUs</a></td></tr>\n", qx.OutURL(), NOut1, qx.Units,
            NOut2);
            qx.Units--;
        }

        // navigate architectures
        fprintf(out, "<tr>");
        CoreType csave = qx.Type;
        if (csave != RISC) {
            qx.Type = RISC;
            fprintf(out, "<td align=center><a href=%s>%sRISC</a></td>", qx.OutURL(), NOut1, NOut2);
        }
        else
            fprintf(out, "<td align=center>%sRISC</td>", NOut1, NOut2);

        if (csave != VLIW) {

```

```

        qx.Type = VLIW;
        fprintf(out, "<td align=center><a href=%s>%sVLIW%</a></td>", qx.OutURL(), NOut1, NOut2);
    }
    else
        fprintf(out, "<td align=center>%sVLIW%</td>", NOutly, NOut1, NOut2);

    if (csave != RED) {
        qx.Type = RED;
        fprintf(out, "<td align=center><a href=%s>%sRED%</a></td>", qx.OutURL(), NOut1, NOut2);
    }
    else
        fprintf(out, "<td align=center>%sRED%</td>", NOutly, NOut1, NOut2);

    if (csave != NCUBE) {
        qx.Type = NCUBE;
        fprintf(out, "<td align=center><a href=%s>%snCUBE%</a></td>", qx.OutURL(), NOut1, NOut2);
    }
    else
        fprintf(out, "<td align=center>%snCUBE%</td>", NOutly, NOut1, NOut2);
    qx.Type = csave;

    fprintf(out, "</tr>\n");

    fprintf(out, "</td></tr></table></table><p>\n");
    fprintf(out, "</td></tr>\n");
    fprintf(out, "</table>\n");
    fprintf(out, "\n");
}

Technology &DRAMTech = y.DRAMProduction;
double DRAMSizeSqMM = DRAMTech.MaxChipSize();
double DRAMBitsCm = DRAMTech.GBitsCm();
double DRAMCostPerBit = DRAMTech.Cost();
double BitsDRAM = DRAMSizeSqMM / 100.0 * DRAMBitsCm * 1024. * 1024. * 1024.;
double DRAMCost = BitsDRAM * DRAMCostPerBit / 1000000. / 100.;

Technology &CustomChipTech = y.ASIC;
double CustomChipSqMM = CustomChipTech.MaxChipSize();
double CustomChipMTransistorCellSize = CustomChipTech.MaxChipSize() / (CustomChipTech.MaxFunctionsPerChip() * Realization);

// Technology &MPUTech = y.HighPerformanceMPU;
// double MPCost = MPUTech.Cost() * MPUTech.MaxFunctionsPerChip() / 100.;

// these will be the chips
Chip CPUChip; // PIM, Blue Light, or standard CPU
Chip MemChip; // standard DRAM or unused
Chip RouterChip; // wormhole router or unused

Picture *Table;

// engineering parameters for a PIM with a RISC or VLIW CPU
if (qx.Type == RISC || qx.Type == VLIW) {
    CPUChip.Name = "PIM";
    CPUChip.SetTech(&CustomChipTech);
    CPUChip.Number = 1;

    CPUChip.ClkMHz = CustomChipTech.LocalClock();
    CPUChip.FLOPS = CPUChip.ClkMHz * qx.Units * (qx.Type == VLIW ? 2 : 1) * 1e6;
    CPUChip.CPUCores = qx.Units;

    CPUChip.IOPads3d = (int)(CustomChipTech.Pads() / 6.);
    CPUChip.IOBandwidth3d = CustomChipTech.ChipToBoardFast() * CPUChip.IOPads3d / 8.0 * 1000000.;

    double CPUSizeSqMM = (qx.Type == VLIW ? 12000000 : 3000000) / 1000000.0 * qx.Units * CustomChipMTransistorCellSize;

    // calculate max DRAM area
    double FlopsFromIOBytes = CPUChip.IOBandwidth3d / IO_BytesPerSecondPerFlop;
    double BytesDRAMFromIOBytes = FlopsFromIOBytes * RAM_BytesPerFlop;
    double BitsDRAMFromIOBytes = BytesDRAMFromIOBytes * 8;
    double DRAMSizeSqMMFromIOBytes = BitsDRAMFromIOBytes * DRAMTech.CellArea() / 1000000.;

    double DRAMSizeSqMM = CustomChipSqMM - CPUSizeSqMM;
    if (DRAMSizeSqMM < 0.0) DRAMSizeSqMM = 0.0;
    if (DRAMSizeSqMM > DRAMSizeSqMMFromIOBytes)
        DRAMSizeSqMM = DRAMSizeSqMMFromIOBytes;

    CPUChip.SqMM = CPUSizeSqMM + DRAMSizeSqMM; // update this parameter

    double OBitsDRAM = DRAMSizeSqMM * 1000000.0 / DRAMTech.CellArea();
    double BitsDRAM = DRAMSizeSqMM / 100 * DRAMTech.GBitsCm() * 1e9;
    CPUChip.BytesDRAM = BitsDRAM / 8.0;

    CPUChip.BusBandwidth = CPUChip.FLOPS * RAM_BytesPerSecondPerFlop;

    // derate
    double DeratedFlops = CPUChip.FLOPS;
    if (DeratedFlops > CPUChip.IOBandwidth3d / IO_BytesPerSecondPerFlop)
        DeratedFlops = CPUChip.IOBandwidth3d / IO_BytesPerSecondPerFlop;
    if (DeratedFlops > CPUChip.BytesDRAM / RAM_BytesPerFlop)
        DeratedFlops = CPUChip.BytesDRAM / RAM_BytesPerFlop;
    if (DeratedFlops > CPUChip.BusBandwidth / RAM_BytesPerSecondPerFlop)
        DeratedFlops = CPUChip.BusBandwidth / RAM_BytesPerSecondPerFlop;
    DeratedFlops = CPUChip.FLOPS;

    CPUChip.IOBandwidth3d = DeratedFlops * IO_BytesPerSecondPerFlop;
    CPUChip.IOPads3d = 1 + (int)(CPUChip.IOBandwidth3d / 1000000. * 8. / CustomChipTech.ChipToBoardFast());

    CPUChip.BytesDRAM = DeratedFlops * RAM_BytesPerFlop;
    DRAMSizeSqMM = CPUChip.BytesDRAM * 8. * DRAMTech.CellArea() / 1000000.;

    DollarsPerNode = CPUChip.CostPerChip;

    Table = new PIMPicture();
    Table->Set(out, qx.Units, 1, CPUSizeSqMM, DRAMSizeSqMM, "cpu", "dram", "pad");
    if ((CPUChip.BytesDRAM + MemChip.BytesDRAM) <= 0.0)
        rval = 1;
}

// engineering parameters for an ASCII Red style node
else if (qx.Type == RED) {
    CPUChip.Name = "CPU";
    MemChip.Name = "DRAM";
    RouterChip.Name = "Wormhole";
}

```

```

// Divide I/O pins into 6 IPC links plus a memory interface
CPUChip.SetTech(&MPUTech);
MemChip.SetTech(&DRAMTech);
RouterChip.SetTech(&CustomChipTech);
CPUChip.Number = qx.Units;
CPUChip.ClkMHz = MPUTech.LocalClock() * Realization;

// estimate performance for a state-of-the art MPU
// assume some number of single issue cores @ 6 million transistors or double issue cores @ 30 million
double cs = MPUTech.HighPerformanceCoreSize();
CPUChip.FLOPS = MPUTech.LocalClock() * Realization * 1000000.;
if (cs > 40) {
    CPUChip.CPUCores = (int)cs/30;
    CPUChip.FLOPS *= CPUChip.CPUCores * 2;
}
else {
    CPUChip.CPUCores = (int)cs/6;
    CPUChip.FLOPS *= CPUChip.CPUCores;
}

RouterChip.IOPads3d = (int)(CustomChipTech.Pads()/7.);
RouterChip.MemPads = (int)(CustomChipTech.Pads() - RouterChip.IOPads3d * 6);
RouterChip.IOBandwidth3d = CustomChipTech.ChipToBoardFast() * Realization * RouterChip.IOPads3d * BUSFACTOR / 8.0 *
1000000.;

RouterChip.CostPerChip = 500.00;
RouterChip.Number = 1;
// double MaxFLOPSFromIO = RouterChip.IOBandwidth3d / IO_BytesPerSecondPerFlop;

CPUChip.MemPads = (int)MPUTech.Pads();
CPUChip.BusBandwidth = CPUChip.MemPads * MPUTech.ChipToBoardFast() * Realization * BUSFACTOR / 8. * 1000000.;

MemChip.MemPads = (int)DRAMTech.Pads();
MemChip.BusBandwidth = MemChip.MemPads * MPUTech.ChipToBoardFast() * Realization * BUSFACTOR / 8. * 1000000.;
MemChip.BytesDRAM = BitsDRAM / 8.0;
// double MaxFLOPSFromBus = min(CPUChip.BusBandwidth, MemChip.BusBandwidth) / RAM_BytesPerSecondPerFlop;

double DeratedFlops = 0.0;
{
    double BestCost = 1e15;
    for (int t = 0; t < 256; t++) {
        DollarsPerNode = CPUChip.CostPerChip * qx.Units + DRAMCost * t + RouterChip.CostPerChip;

        double df = CPUChip.FLOPS * qx.Units;
        if (df > RouterChip.IOBandwidth3d / IO_BytesPerSecondPerFlop)
            df = RouterChip.IOBandwidth3d / IO_BytesPerSecondPerFlop;
        if (df > MemChip.BytesDRAM * t / RAM_BytesPerFlop)
            df = MemChip.BytesDRAM * t / RAM_BytesPerFlop;
        if (df > CPUChip.BusBandwidth / RAM_BytesPerSecondPerFlop)
            df = CPUChip.BusBandwidth / RAM_BytesPerSecondPerFlop;
        if (df > MemChip.BusBandwidth * t / RAM_BytesPerSecondPerFlop)
            df = MemChip.BusBandwidth * t / RAM_BytesPerSecondPerFlop;
        if (df > 0.0 && BestCost > DollarsPerNode / df) {
            MemChip.Number = t;
            BestCost = DollarsPerNode / df;
            DeratedFlops = df;
        }
    }
}

DollarsPerNode = CPUChip.CostPerChip * qx.Units + DRAMCost * MemChip.Number + RouterChip.CostPerChip;

RouterChip.IOBandwidth3d = DeratedFlops * IO_BytesPerSecondPerFlop;
RouterChip.IOPads3d = (int)(RouterChip.IOBandwidth3d / 1000000. * 8. / BUSFACTOR / MPUTech.ChipToBoardFast() /
Realization);

Table = new RedPicture();
Table->Set(out, qx.Units, MemChip.Number, MPUTech.MaxChipSize(), DRAMSizeSqMM, "cpu", "DRAM", "pad");
}

// engineering parameters for an ASCII Blue Light style node
else {
    CPUChip.Name = "ASIC";
    MemChip.Name = "DRAM";

    CPUChip.SetTech(&CustomChipTech);
    MemChip.SetTech(&DRAMTech);
    CPUChip.Number = 1;
    CPUChip.ClkMHz = CustomChipTech.LocalClock() * Realization;
    CPUChip.FLOPS = CPUChip.ClkMHz * qx.Units * 2. * 1000000.;
    CPUChip.CPUCores = qx.Units;

    double FracPinsToMemory = RAM_BytesPerSecondPerFlop / (max(IO_BytesPerSecondPerFlop * 6., IO_BytesPerSecondPerFlopAll) +
RAM_BytesPerSecondPerFlop);
    double FracPinsToIO = 1. - FracPinsToMemory;

    CPUChip.IOPads3d = (int)(CustomChipTech.Pads()*FracPinsToIO/6. + .5);
    CPUChip.IOBandwidth3d = CustomChipTech.ChipToBoardFast() * Realization * CPUChip.IOPads3d / 8.0 * 1000000.;
    CPUChip.MemPads = (int)(CustomChipTech.Pads()*FracPinsToMemory + .5);
    CPUChip.BusBandwidth = CustomChipTech.Pads() * CustomChipTech.ChipToBoardFast() * Realization * BUSFACTOR *
FracPinsToMemory / 8.0 * 1000000.;

    MemChip.MemPads = (int)DRAMTech.Pads();
    MemChip.BusBandwidth = MemChip.MemPads * MPUTech.ChipToBoardFast() * Realization * BUSFACTOR / 8. * 1000000.;
    MemChip.BytesDRAM = BitsDRAM / 8.0;

    {
        double BestCost = 1e15;
        for (int t = 0; t < 256; t++) {
            DollarsPerNode = CPUChip.CostPerChip + t * DRAMCost;
            double df = CPUChip.FLOPS;
            if (df > CPUChip.IOBandwidth3d / IO_BytesPerSecondPerFlop)
                df = CPUChip.IOBandwidth3d / IO_BytesPerSecondPerFlop;
            if (df > MemChip.BytesDRAM * t / RAM_BytesPerFlop)
                df = MemChip.BytesDRAM * t / RAM_BytesPerFlop;
            if (df > CPUChip.BusBandwidth / RAM_BytesPerSecondPerFlop)
                df = CPUChip.BusBandwidth / RAM_BytesPerSecondPerFlop;
            if (df > MemChip.BusBandwidth * t / RAM_BytesPerSecondPerFlop)
                df = MemChip.BusBandwidth * t / RAM_BytesPerSecondPerFlop;
            if (BestCost > DollarsPerNode / df) {
                MemChip.Number = t;
                BestCost = DollarsPerNode / df;
            }
        }
    }
}
}

```

```

DollarsPerNode = CPUChip.CostPerChip + MemChip.Number * DRAMCost;

// if the specified number of units exceeds the capacity of the ASIC, drop out of the optimization
if (qx.Units * 30. > CustomChipSqMM / CustomChipMTransistorCellSize)
    DollarsPerNode = 1e200;

Table = new nCUBEPicture();
Table->Set(out, 1, MemChip.Number, CustomChipTech.MaxChipSize(), DRAMTech.MaxChipSize(), "cpu", "dram", "pad");
}

// identify bottleneck and derate FLOPS appropriately
char *why = "FLOPS";
double DeratedFlops = CPUChip.FLOPS * CPUChip.Number;
if (DeratedFlops > (CPUChip.IOBandwidth3d + RouterChip.IOBandwidth3d) / IO_BytesPerSecondPerFlop) {
    DeratedFlops = (CPUChip.IOBandwidth3d + RouterChip.IOBandwidth3d) / IO_BytesPerSecondPerFlop;
    why = "IO";
}
if (DeratedFlops > (CPUChip.BytesDRAM + MemChip.BytesDRAM * MemChip.Number) / RAM_BytesPerFlop) {
    DeratedFlops = (CPUChip.BytesDRAM + MemChip.BytesDRAM * MemChip.Number) / RAM_BytesPerFlop;
    why = "RAM";
}
if (DeratedFlops > CPUChip.BusBandwidth / RAM_BytesPerSecondPerFlop) {
    DeratedFlops = CPUChip.BusBandwidth / RAM_BytesPerSecondPerFlop;
    why = "CPU Bus";
}
if (MemChip.Number > 0 && DeratedFlops > MemChip.BusBandwidth * MemChip.Number / RAM_BytesPerSecondPerFlop) {
    DeratedFlops = MemChip.BusBandwidth * MemChip.Number / RAM_BytesPerSecondPerFlop;
    why = "Mem Bus";
}
UnitsPerPetaFlop = qx.PerformanceTarget/DeratedFlops;

if (out != NULL) {
fprintf(out, "<table border=\0\ width=\140\ valign=\top\>\n");
fprintf(out, "<tr valign=\top\ align=\center\><td width=\114\ valign=\top\>\n");
fprintf(out, "<!------- #1 - secondary navigation----->\n");
//
fprintf(out, "<font color=white>Nav text2<br></font>");
fprintf(out, "<table align=center><tr><td align=center>\n");
//
fprintf(out, "%s<br>"
"%0.1f nodes<br>"
"%s FLOPS<br>"
"limited by %s<br>"
"GreekSuffix(DollarsPerNode * UnitsPerPetaFlop),
UnitsPerPetaFlop, GreekSuffix(qx.PerformanceTarget), why, NOut2);
//
int skew = 3;
int thsize = 50;
if (1) {
double Cost = DollarsPerNode * UnitsPerPetaFlop;

double x = sqrt(Cost/7.75e6);
double scale = thsize / (x + 1);

fprintf(out, "<table align=center><tr><td valign=bottom>\n");
fprintf(out, "<table><tr><td align=center><img src=mon.gif width=%d height=%d></td></tr><tr><td
align=center>%sSystem<br>Cost</td></tr></table>\n", (int)(scale * x), (int)(skew * scale * x), NOut1, NOut2);
fprintf(out, "</td><td valign=bottom>");
fprintf(out, "<table><tr><td align=center><img src=mon.gif width=%d height=%d></td></tr><tr><td
align=center>%sRed<br>Storm</td></tr></table>\n", (int)(scale), (int)(skew * scale), NOut1, NOut2);
fprintf(out, "</td></tr></table>");
}
if (1) {
double TotalW = 0.0;
if (CPUChip.Number > 0)
    TotalW += CPUChip.Number * CPUChip.Power();
if (MemChip.Number > 0)
    TotalW += MemChip.Number * MemChip.Power();
if (RouterChip.Number > 0)
    TotalW += RouterChip.Number * RouterChip.Power();
TotalW *= UnitsPerPetaFlop;

double x = sqrt(TotalW/1.55e6);
double scale = thsize / (x + 1);

fprintf(out, "<table align=center><tr><td valign=bottom>\n");
fprintf(out, "<table><tr><td align=center><img alt=%sW src=pw.gif width=%d height=%d></td></tr><tr><td
align=center>%sTotal<br>Power</td></tr></table>\n", GreekSuffix(TotalW), (int)(scale * x), (int)(skew * scale * x), NOut1, NOut2);
fprintf(out, "</td><td valign=bottom>");
fprintf(out, "<table><tr><td align=center><img alt=%sW src=pw2.gif width=%d height=%d></td></tr><tr><td
align=center>%sRed<br>Storm</td></tr></table>\n", "1.55M", (int)(scale), (int)(skew * scale), NOut1, NOut2);
fprintf(out, "</td></tr></table>");
}
}
if (0) {
double Uptime = 40.0 * 100 / UnitsPerPetaFlop;

double x = sqrt(Uptime);
double scale = thsize / (x + 1);
scale *= 1.5;

fprintf(out, "<table align=center><tr><td valign=bottom>\n");
fprintf(out, "<table><tr><td align=center><img alt=%11f H\ src=time.gif width=%d
height=%d></td></tr><tr><td align=center>%sTime To<br>Failure</td></tr></table>\n", Uptime, (int)(scale * x), (int)(scale * x * 404 / 462),
NOut1, NOut2);
fprintf(out, "</td><td valign=bottom>");
fprintf(out, "<table><tr><td align=center><img alt=%s\ src=time.gif width=%d height=%d></td></tr><tr><td
align=center>%sRed<br>Storm</td></tr></table>\n", "40 H", (int)(scale), (int)(scale * 404 / 462), NOut1, NOut2);
fprintf(out, "</td></tr></table>");
}
}

fprintf(out, "</td></tr></table></table>\n");
//
fprintf(out, "<font color=white>Nav text2<br></font>");
fprintf(out, "</td></tr>\n");
fprintf(out, "\n");
fprintf(out, "<tr valign=\top\ align=\center\><td width=\114\ valign=\top\>\n");
fprintf(out, "<!------- #2 - secondary navigation----->\n");
//
fprintf(out, "<a href=\http://www.sandia.gov/partnerships/\>\n");
//
fprintf(out, "<font color=white>Nav text3</font>");
fprintf(out, "</td></tr></table>\n");
fprintf(out, "\n");
fprintf(out, "</td>\n");
fprintf(out, "<td valign=\top\ align=\center\ width=\100%\>\n");

```

```

printf(out, "\n");
printf(out, "<table border='0' width='445' align='center' valign='top'>\n");
printf(out, "<tr width='445'><td width='445'>\n");
printf(out, "\n");
printf(out, "<table border='0' width='100%%' align='center' valign='top' cellspacing='0' cellpadding='0'>\n");
printf(out, "<tr>\n");
printf(out, "<td valign='top'>\n");
printf(out, "<!-- top banner graphic/text goes here ----->\n");
printf(out, "<img src='petaflopsplanner.gif' width='183' height='26' hspace='0' vspace='4' alt='Programs'></td>\n");
printf(out, "\n");
printf(out, "<td valign='top' align='right'>\n");
printf(out, "<a href='http://www.sandia.gov/Main.html'><img border='0' src='logo.gif' align='center' width='151'
hspace='0' height='60' vspace='0' alt='Sandia National Laboratories'></a></td></tr>\n");
printf(out, "<tr><td colspan='2'>\n");
printf(out, "<hr>\n");
printf(out, "</td></tr>\n");
printf(out, "</table>\n");
printf(out, "\n");
printf(out, "<center>\n");
printf(out, "<!-- body begins here ----->\n");
printf(out, "<table border='0' width='100%%' align='top' cellspacing='0' cellpadding='0'>\n");
printf(out, "<tr>\n");
printf(out, "<td>\n");
//printf(out, "body");
printf(out, "<center>%sSilicon Area Floorplan</center>\n", Index1a, Index2);

Table->Print();

int nn = (int)pow(UnitsPerPetaFlop, 1./3.);
if (0 && nn < 40) {
    int n = nn/2;
    if (n == 0) n = 1;

    int w = 12;
    int h = 6;

    char *b = "x";
    printf(out, "<table align=center><tr><th>%s x %d x %d System</th></tr>", Index1, nn, nn, Index2);
    printf(out, "<tr><td>");
    printf(out, "<table border=0 cellpadding=0 cellspacing=0 align=center>");
    if (1) for (int i = 0; i < n; i++) {
        printf(out, "<tr>");
        if (1) for (int j = 0; j < n - i - 1; j++)
            printf(out, "<td><img src=%sw.gif width=%d height=%d</td>", b, w, h);
        printf(out, "<td><img src=%sa.gif width=%d height=%d</td>", b, w, h);
        if (1) for (int j = 0; j < n - 1; j++)
            printf(out, "<td><img src=%sb.gif width=%d height=%d</td>", b, w, h);
        printf(out, "<td><img src=%sc.gif width=%d height=%d</td>", b, w, h);
        if (1) for (int j = 0; j < i; j++)
            printf(out, "<td><img src=%se.gif width=%d height=%d</td>", b, w, h);
        printf(out, "</tr>\n");
    }
    if (1) for (int i = 0; i < n; i++) {
        printf(out, "<tr>");
        if (1) for (int j = 0; j < n; j++)
            printf(out, "<td><img src=%sf.gif width=%d height=%d</td>", b, w, h);
        if (1) for (int j = 0; j < n - i - 1; j++)
            printf(out, "<td><img src=%se.gif width=%d height=%d</td>", b, w, h);
        printf(out, "<td><img src=%sg.gif width=%d height=%d</td>", b, w, h);
        printf(out, "</tr>\n");
    }
    printf(out, "</table>\n");
    printf(out, "</td></tr></table>\n");
}

printf(out, "<table border align=center><tr><td valign=top>%s\n", Index1);

#define COST 0
#define SAGE 0
#define EXTPERF 0
#define POWER 1

#if COST
printf(out, "<h2>Cost</h2>\n"); // {
if (CPUChip.Number > 0) printf(out, "$%.21f %s (%d x $%.21f)<br>\n", CPUChip.Number * CPUChip.CostPerChip,
CPUChip.Name, CPUChip.CostPerChip);
if (MemChip.Number > 0) printf(out, "$%.21f %s (%d x $%.21f)<br>\n", MemChip.Number * MemChip.CostPerChip,
MemChip.Name, MemChip.CostPerChip);
if (RouterChip.Number > 0) printf(out, "$%.21f %s (%d x $%.21f)<br>\n", RouterChip.Number * RouterChip.CostPerChip,
RouterChip.Name, RouterChip.CostPerChip);
printf(out, "-----<br>$.21f chip per node total<br>\n", CPUChip.Number * CPUChip.CostPerChip + MemChip.Number
* MemChip.CostPerChip + RouterChip.Number * RouterChip.CostPerChip); // }
#endif

#if SAGE
printf(out, "<h2>Sage Performance</h2>\n"); // {
// parameters
double E = (MemChip.Number * MemChip.BytesDRAM + CPUChip.BytesDRAM)/100000; // points per PE
double P = UnitsPerPetaFlop; // number of PEs
double L = pow(E * P, .3333); // points on side of cube
printf(out, "%s points per PE; %s PEs; %s points per side<br>\n", GreekSuffix(E), GreekSuffix(P), GreekSuffix(L));

double SurfaceZ = min(L*L, E/2); // points on Z surface
double SurfaceY = 2*L; // points on Y surface
double SurfaceX = 4; // points on X surface
printf(out, "%s x %s x %s slab<br>\n", GreekSuffix(SurfaceY), GreekSuffix(SurfaceZ), GreekSuffix(SurfaceX));

double PSMP = qx.Units; // processors in SMP
double CL = 1; // communications links per node
printf(out, "%s processors per SMP; %s links between PEs<br>\n", GreekSuffix(PSMP), GreekSuffix(CL));

// MPI Latency at 2 nanoseconds plus 5000 clock cycles
// adjust for distance @ 2 ns/foot plus 20 clock cycles per hop
double MPLatency = 2e-9 + 5000/CPUChip.ClkMHz/1e6;
double MPIOBandwidth = RouterChip.IOBandwidth/3 + CPUChip.IOBandwidth/3;

// Inter CPU latency at 2000 clock cycles
double LocalLatency = 2000/CPUChip.ClkMHz/1e6;

// latency for a message of size S
#define Lc1(S) ((S)<64 ? 4.8e-6 : (S)<=256 ? 4.9e-6 : (S)<=8192 ? 13.5e-6 : 23.2e-6)

```

```

#define Lc2(S) ((S)<64 ? 6.10e-6 : (S)<=512 ? 6.44e-6 : 13.8e-6)
#define Lc(S, P) ((P)<=4 ? Lc1(S) : Lc2(S))

// time per byte for a message of size S
#define Bc1inv(S) ((S)<64 ? 0 : (S)<=256 ? 13.9e-9 : (S)<=8192 ? 1.04e-9 : 1.37e-9)
#define Bc2inv(S) ((S)<64 ? 0 : (S)<=512 ? 12.2e-9 : 8.30e-9)
#define Bcinv(S, P) ((P)<=4 ? Bc1inv(S) : Bc2inv(S))

double MPIReal8 = 8;
double MPIInt = 4;

// Tcomp is the grid time
// someday this should distinguish between cache and main memory
#define Tcomp(E) ((.36/13500.*CPUChip.ClkMHz/500)*E)

// Memory contention -- what is this?
#define Tmem(P) ((P) <= 2 ? 1.8e-6 : 4.8e-6)

// formulas
// communications time of a message of size S
#define Tcomm(S, P) (Lc(S, P) + S * Bcinv(S, P))

// topology dependent: not logarithmic in a mesh
#define Tallreduce(P) (120*2*log(P)/log(2)*Tcomm(4, P))

#define Tmemcon(P, E) (E)*Tmem(P)

// this is something like the number of PEs on the surface of a subgrid
// these could all be contending for a grid link
#define PESurface 12

#define C(P, E) min(max(L*L/CL/PESurface, 1), PSMP/CL)

#define TGSComm(P, E) (C(P, E) * \
    (160*Tcomm(Surface2*MPIReal8, P) + \
    17*Tcomm(Surface2*MPIInt, P) + \
    160*Tcomm(SurfaceY*MPIReal8, P) + \
    17*Tcomm(SurfaceY*MPIInt, P) + \
    160*Tcomm(SurfaceX*MPIReal8, P) + \
    17*Tcomm(SurfaceX*MPIInt, P))

#define Tcycle(P, E) Tcomp(E) + Tmemcon(P, E) + TGSComm(P, E) + Tallreduce(P)
printf(out, "Tcomp(%s) = %s<br>\n", GreekSuffix(E), GreekSuffix(Tcomp(E)));
printf(out, "Tmemcon(%s, %s) = %s<br>\n", GreekSuffix(P), GreekSuffix(E), GreekSuffix(Tmemcon(P, E)));
printf(out, "TGSComm(%s, %s) = %s<br>\n", GreekSuffix(P), GreekSuffix(E), GreekSuffix(TGSComm(P, E)));
printf(out, "Tallreduce(%s) = %s<br>\n", GreekSuffix(P), GreekSuffix(Tallreduce(P)));
double aa=Tcycle(P, E);
printf(out, "Tcycle=%s<br>\n", GreekSuffix(aa));
printf(out, "efficiency=%.01f%%<br>\n", Tcomp(E)/aa*100);

#endif
// ( // )
#if EXTPERF
    fprintf(out, "<h2>Application Performance</h2>\n");

    FILE *f = fopen("arch.bat", "w+");
    if (f == NULL)
        fprintf(out, "couldn't write arch.bat<br>\n");
    else {
        fprintf(f, "dir/b > arch.out\n");

        fprintf(f, "rem <bytes>%5.1e</bytes>\n", (MemChip.Number * MemChip.BytesDRAM + CPUChip.BytesDRAM));
        fprintf(f, "rem <nodes>%5.1e</nodes>\n", UnitsPerPetaFlop);
        fprintf(f, "rem <psmp>%d</psmp>\n", qx.Units);
        fprintf(f, "rem <mpilatency>%5.1e</mpilatency>\n", 2e-9 + 5000/CPUChip.ClkMHz/1e6);
        fprintf(f, "rem <mpibytetime>%5.1e</mpibytetime>\n", RouterChip.IOBandwidth3d + CPUChip.IOBandwidth3d);

        fclose(f);

        UINT rc = WinExec("arch.bat", SW_SHOWNORMAL);
        if (rc <= 31)
            fprintf(out, "error: return code %d from subjob<br>\n", rc);
        else {
            f = fopen("arch.out", "r");
            if (f == NULL)
                fprintf(out, "couldn't read arch.out<br>\n");
            else {
                fprintf(out, "<pre>\n");
                char buf[500];
                int r;
                while ((r = fread(buf, 1, 500, f)) > 0) {
                    fwrite(buf, 1, r, out);
                }
                fprintf(out, "</pre>\n");

                if (fseek(f, 0, SEEK_END) != 0)
                    fprintf(out, "couldn't seek arch.out<br>\n");
                else {
                    int len = ftell(f);
                    fprintf(out, "successfully read %d bytes<br>\n", len);
                }
            }
        }
    }
    fclose(f);
}
// }

#endif
// ( // )
#if POWER
    fprintf(out, "<h2>Power</h2>\n");

    double TotalW = 0.0;
    if (CPUChip.Number > 0) {
        fprintf(out, "%sW %s (%d x %sW)<br>\n", GreekSuffix(CPUChip.Number * CPUChip.Power()), CPUChip.Name,
        CPUChip.Number, GreekSuffix(CPUChip.Power()));
        TotalW += CPUChip.Number * CPUChip.Power();
    }
    if (MemChip.Number > 0) {
        fprintf(out, "%sW %s (%d x %sW)<br>\n", GreekSuffix(MemChip.Number * MemChip.Power()), MemChip.Name,
        MemChip.Number, GreekSuffix(MemChip.Power()));
        TotalW += MemChip.Number * MemChip.Power();
    }
    if (RouterChip.Number > 0) {
        fprintf(out, "%sW %s (%d x %sW)<br>\n", GreekSuffix(RouterChip.Number * RouterChip.Power()),
        RouterChip.Name, RouterChip.Number, GreekSuffix(RouterChip.Power()));
        TotalW += RouterChip.Number * RouterChip.Power();
    }
}

```

```

    }
    fprintf(out, "-----<br>%2lfW per node total<br>\n", TotalW);
    fprintf(out, "%5W IC power for %d nodes<br>\n", GreekSuffix(TotalW * (int)UnitsPerPetaFlop), (int)UnitsPerPetaFlop);
    fprintf(out, "%5W est. total (2x)<br>\n", GreekSuffix(TotalW * (int)UnitsPerPetaFlop * 2));
// }

    fprintf(out, "%s</td><td valign=top>%s\n", Index2, Index1);

CPUChip.Print(out);

    fprintf(out, "%s</td></tr><tr><td valign=top>%s\n", Index2, Index1);

MemChip.Print(out);

    fprintf(out, "%s</td><td valign=top>%s\n", Index2, Index1);

RouterChip.Print(out);

    fprintf(out, "%s</td></tr></table>\n", Index2);

//
    fprintf(out, "</td></tr>\n"); // basic page layout
//
    fprintf(out, "</table></td></tr></table>\n"); // basic page layout
    fprintf(out, "<br clear=all>\n");

    fprintf(out, "</td></tr>\n");
    fprintf(out, "</table>\n");
    fprintf(out, "</center>\n");
    fprintf(out, "\n");
    fprintf(out, "<!-- body ends here ----->\n");
    fprintf(out, "</td></tr></table>\n");
    fprintf(out, "\n");
    fprintf(out, "</td></tr></table>\n");
    fprintf(out, "\n");
    fprintf(out, "chr width=\"100%%>\n");
    fprintf(out, "\n");
    fprintf(out, "<table align=\"top\" border=\"0\" width=\"100%%>\n");
    fprintf(out, "<tr align=\"center\">\n");
    fprintf(out, "<td valign=\"top\" width=\"140\">\n");
    fprintf(out, "<table border=\"0\" width=\"140\">\n");
    fprintf(out, "<tr><td align=\"center\" width=\"120\" valign=\"top\">\n");
    fprintf(out, "<font size=\"-1\" color=\"#FFFFFF\">\n");
    fprintf(out, "<br></font>\n");
    fprintf(out, "</td>\n");
    fprintf(out, "<td width=\"20\">\n");
    fprintf(out, "<br>\n");
    fprintf(out, "</td></tr></table>\n");
    fprintf(out, "\n");
    fprintf(out, "</td>\n");
    fprintf(out, "\n");
    fprintf(out, "<td valign=\"top\" align=\"center\" width=\"100%%>\n");
    fprintf(out, "\n");
    fprintf(out, "<table border=\"0\" width=\"100%%\" align=\"center\" valign=\"top\">\n");
    fprintf(out, "<tr valign=top><td>\n");
    fprintf(out, "<font size=\"-1\"><center>\n");
    fprintf(out, "<a href=\"#TOP\">Back to top of page</a> || \n");
    fprintf(out, "<a href=\"http://www.sandia.gov/feedback.htm\">Questions and Comments</a> || \n");
    fprintf(out, "<a href=\"http://www.sandia.gov/dis.htm\">Acknowledgment and Disclaimer</a></center></font>\n");
    fprintf(out, "</td></tr></table>\n");
    fprintf(out, "\n");
    fprintf(out, "</td></tr></table>\n");
    fprintf(out, "\n");
    fprintf(out, "</html>\n");
    fprintf(out, "\n");
}

delete Table;

return rval;
}

int Summary(FILE *index, Query &qx, int doit) {
    fprintf(index, "<html><head><title>Petaflops Planner</title></head>\n");
    fprintf(index, "<body background=\"bkgnd.gif\" text=\"#000000\" link=\"#003366\" vlink=\"#cc0033\" alink=\"#000000\">\n");
    fprintf(index, "<a name=\"TOP\"></a>\n");
    fprintf(index, "<table border=\"0\" width=\"100%%\">\n");
    fprintf(index, "<tr valign=\"top\"><td>\n");
    fprintf(index, "<table border=\"0\" width=\"140\" valign=\"top\">\n");
    fprintf(index, "<tr valign=\"top\"><td width=\"140\" valign=\"top\">\n");
    fprintf(index, "\n");
//
    fprintf(index, "1 nav");
    fprintf(index, "</td></tr>\n");
    fprintf(index, "</table>\n");
    fprintf(index, "\n");
    fprintf(index, "<table border=\"0\" width=\"140\" valign=\"top\">\n");
    fprintf(index, "<tr valign=\"top\" align=\"center\"><td width=\"114\" valign=\"top\">\n");
    fprintf(index, "<!-- #1 - secondary navigation----->\n");
//
    fprintf(index, "2 nav");
    fprintf(index, "<a href=index.htm target=query>%sIndex&s</a><br>", NOut1, NOut2);
    fprintf(index, "<a href=help.htm>%sHelp&s</a>", NOut1, NOut2);
    fprintf(index, "</td></tr>\n");
    fprintf(index, "\n");
    fprintf(index, "<tr valign=\"top\" align=\"center\"><td width=\"114\" valign=\"top\">\n");
    fprintf(index, "<!-- #2 - secondary navigation----->\n");
//
    fprintf(index, "3 nav");
    fprintf(index, "</td></tr></table>\n");
    fprintf(index, "\n");
    fprintf(index, "</td>\n");
    fprintf(index, "<td valign=\"top\" align=\"center\" width=\"100%%\">\n");
    fprintf(index, "\n");
    fprintf(index, "<table border=\"0\" width=\"445\" align=\"center\" valign=\"top\">\n");
    fprintf(index, "<tr width=\"445\"><td width=\"445\">\n");
    fprintf(index, "\n");
    fprintf(index, "<table border=\"0\" width=\"100%%\" align=\"center\" valign=\"top\" cellspacing=\"0\" cellpadding=\"0\">\n");
    fprintf(index, "<tr>\n");
    fprintf(index, "<td valign=\"top\">\n");
    fprintf(index, "<!-- top banner graphic/text goes here ----->\n");
    fprintf(index, "<img src=\"petaflopsplanner.gif\" width=\"183\" height=\"26\" hspace=\"0\" vspace=\"4\" alt=\"Programs\"></td>\n");
    fprintf(index, "\n");
    fprintf(index, "<td valign=\"top\" align=\"right\">\n");
    fprintf(index, "<a href=\"http://www.sandia.gov/Main.html\"><img border=\"0\" src=\"logo.gif\" align=\"center\" width=\"151\" hspace=\"0\" height=\"60\" vspace=\"0\" alt=\"Sandia National Laboratories\"></a></td></tr>\n");
    fprintf(index, "<tr><td colspan=\"2\">\n");

```

```

fprintf(index, "<hr>\n");
fprintf(index, "</td></tr>\n");
fprintf(index, "</table>\n");
fprintf(index, "\n");
fprintf(index, "<center>\n");
fprintf(index, "\n");
fprintf(index, "!----- body begins here -----!\n");
fprintf(index, "<table border='0' width='100%' valign='top' cellspacing='0' cellpadding='0'\n");
fprintf(index, "<tr>\n");
fprintf(index, "<td>\n");
// fprintf(index, "body");
if (doit != 0) {
    fprintf(index, "<table border=0><tr>\n");

    for (qx.Class = 0; qx.Class < 2; qx.Class++) {

        fprintf(index, "<td>\n");
        fprintf(index, "<table border><tr><th colspan=5>%s</th></tr>"

            "<tr><th>%Year</th><th>%RISC<br>PIM</th><th>%VLIW<br>PIM</th><th>%Red<br>Storm</th><th>%snCUBE<br>BC/L</th></tr>\n",
            Out1, qx.Class == 0 ? "Data Intensive" : "FLOPS Intensive", Out2, Out1, Out2, Out1, Out2, Out1,
            Out2, Out1, Out2, Out1, Out2);
        for (qx.Year = qx.Year1; qx.Year <= qx.Year2; qx.Year += 1.0) {

            fprintf(stderr, "%d ", (int)qx.Year);

            int BestCPUs[4];
            double BestCost[4];
            char *BestURL[4];

            if (1) for (int core = 0; core < 4; core++) {

                qx.Type = core == 0 ? RISC : core == 1 ? VLIW : core == 2 ? RED : NCUBE;

                BestCPUs[core] = 0;
                BestCost[core] = 1e100;
                BestURL[core] = NULL;

                // iterate through units -- PIM CPUs or DRAM chips
                for (qx.Units1 = qx.Units1; qx.Units1 <= qx.Units2; qx.Units1++) {

                    double DollarsPerNode;
                    double UnitsPerPetaFlop;
                    int Error = FloorPlanner(NULL, qx, DollarsPerNode, UnitsPerPetaFlop);

                    if (Error == 0 && BestCost[core] > DollarsPerNode * UnitsPerPetaFlop) {
                        BestCPUs[core] = qx.Units;
                        BestCost[core] = DollarsPerNode * UnitsPerPetaFlop;
                        if (BestURL[core] != NULL) free(BestURL[core]);
                        BestURL[core] = strdup(qx.OutURL());
                    }

                }

            }

            if (1)

                fprintf(index, "<tr><td>%d</td><td align=center>%s<a href=%s target=meef>%d"

                    " (%s)"

                    "</a>%s</td>"

                    "<td align=center>%s<a href=%s target=meef>%d"

                    " (%s)"

                    "</a>%s</td>"

                    "<td align=center>%s<a href=%s target=meef>%d"

                    " (%s)"

                    "</a>%s</td></tr>\n", Out1, (int)qx.Year, Out2,
                    BestCost[0] < BestCost[1] && BestCost[0] < BestCost[2] && BestCost[0] < BestCost[3]

                    GreekSuffix(BestCost[0]),

                    Out2,
                    BestCost[1] <= BestCost[0] && BestCost[1] < BestCost[2] && BestCost[1] <

                    GreekSuffix(BestCost[1]),

                    Out2,
                    BestCost[2] <= BestCost[1] && BestCost[2] <= BestCost[0] && BestCost[2] <

                    GreekSuffix(BestCost[2]),

                    Out2,
                    BestCost[3] <= BestCost[2] && BestCost[3] <= BestCost[1] && BestCost[3] <=

                    GreekSuffix(BestCost[3]),

                    Out2);

            else

                fprintf(index, "<tr><td>%d</td><td align=center>%s<a href=%s target=meef>%d"

                    "<br>(%s)"

                    "</a>%s</td>"

                    "<td align=center>%s<a href=%s target=meef>%d"

                    "<br>(%s)"

                    "</a>%s</td>"

                    "<td align=center>%s<a href=%s target=meef>%d"

                    "<br>(%s)"

                    "</a>%s</td></tr>\n", Out1, (int)qx.Year, Out2,

```

```

BestCost[0] < BestCost[1] && BestCost[0] < BestCost[2] && BestCost[0] < BestCost[3]
? Index1a : Out1, BestURL[0], BestCPUs[0],
BestCost[3] ? Index1a : Out1, BestURL[1], BestCPUs[1],
BestCost[3] ? Index1a : Out1, BestURL[2], BestCPUs[2],
BestCost[0] ? Index1a : Out1, BestURL[3], BestCPUs[3],

    GreekSuffix(BestCost[0]),
    Out2,
    BestCost[1] <= BestCost[0] && BestCost[1] < BestCost[2] && BestCost[1] <
    GreekSuffix(BestCost[1]),
    Out2,
    BestCost[2] <= BestCost[1] && BestCost[2] <= BestCost[0] && BestCost[2] <
    GreekSuffix(BestCost[2]),
    Out2,
    BestCost[3] <= BestCost[2] && BestCost[3] <= BestCost[1] && BestCost[3] <=
    GreekSuffix(BestCost[3]),
    Out2);

    if (1) for (int core = 0; core < 4; core++)
        if (BestURL[core] != NULL)
            free(BestURL[core]);
    }
    fprintf(stderr, "\n");

    fprintf(index, "</table>\n");
    fprintf(index, "</td>\n");
}

fprintf(index, "</tr>\n");
fprintf(index, "<tr><td colspan=2>%sLegend: n ($p) where<br>"
    "n is number of CPU units<br>"
    "$p is dollars to build a %sFLOPS supercomputer<br>%s"
    "%slarge text%s indicates this is the best alternative<br>%s</td></tr>";
    NOut1, GreekSuffix(qx.PerformanceTarget), NOut2, NOut1a, NOut2, NOut1, NOut2);

fprintf(index, "</table>\n");
}

//fprintf(index, "body end");
fprintf(index, "</td></tr>\n");
fprintf(index, "</table>\n");
fprintf(index, "</center>\n");
fprintf(index, "\n");
fprintf(index, "<!-- body ends here -->\n");
fprintf(index, "</td></tr></table>\n");
fprintf(index, "\n");
fprintf(index, "</td></tr></table>\n");
fprintf(index, "\n");
fprintf(index, "<hr width='100%'>\n");
fprintf(index, "\n");
fprintf(index, "<table align='top' border='0' width='100%'>\n");
fprintf(index, "<tr align='center'>\n");
fprintf(index, "<td valign='top' width='140'>\n");
fprintf(index, "<table border='0' width='140'>\n");
fprintf(index, "<tr><td align='center' width='120' valign='top'>\n");
fprintf(index, "<font size='-1' color='FFFFFF'>\n");
fprintf(index, "<br></font>\n");
fprintf(index, "</td>\n");
fprintf(index, "<td width='20'>\n");
fprintf(index, "<br>\n");
fprintf(index, "</td></tr></table>\n");
fprintf(index, "\n");
fprintf(index, "</td>\n");
fprintf(index, "\n");
fprintf(index, "<td valign='top' align='center' width='100%'>\n");
fprintf(index, "\n");
fprintf(index, "<table border='0' width='100%' align='center' valign='top'>\n");
fprintf(index, "<tr valign=top><td>\n");
fprintf(index, "<font size='-1'><center>\n");
fprintf(index, "<a href='#TOP'>Back to top of page</a> || \n");
fprintf(index, "<a href='http://www.sandia.gov/feedback.htm'>Questions and Comments</a> || \n");
fprintf(index, "<a href='http://www.sandia.gov/dis.htm'>Acknowledgment and Disclaimer</a></center></font>\n");
fprintf(index, "</td></tr></table>\n");
fprintf(index, "\n");
fprintf(index, "</td></tr></table>\n");
fprintf(index, "\n");
fprintf(index, "</html>\n");
fprintf(index, "\n");

return 0;
}

int Help(FILE *index) {

    fprintf(index, "<html><head><title>Petaflops Planner Help</title></head>\n");
    fprintf(index, "<body background='bkgrrnd.gif' text='#000000' link='#003366' vlink='#cc0033' alink='#000000'>\n");
    fprintf(index, "<a name='TOP'></a>\n");
    fprintf(index, "<table border='0' width='100%'>\n");
    fprintf(index, "<tr valign='top'><td>\n");
    fprintf(index, "<table border='0' width='140' valign='top'>\n");
    fprintf(index, "<tr valign='top'><td width='140' valign='top'>\n");
    fprintf(index, "\n");
    //    fprintf(index, "1 nav");
    fprintf(index, "</td></tr>\n");
    fprintf(index, "</table>\n");
    fprintf(index, "\n");
    fprintf(index, "<table border='0' width='140' valign='top'>\n");
    fprintf(index, "<tr valign='top' align='center'><td width='114' valign='top'>\n");
    fprintf(index, "<!-- #1 - secondary navigation -->\n");
    //    fprintf(index, "2 nav");
    fprintf(index, "<a href=/index.htm target=query>%sIndex</a><br>", NOut1, NOut2);
    fprintf(index, "<a href=/help.htm>%sHelp</a>", NOut1, NOut2);
    fprintf(index, "</td></tr>\n");
    fprintf(index, "\n");
    fprintf(index, "<tr valign='top' align='center'><td width='114' valign='top'>\n");
    fprintf(index, "<!-- #2 - secondary navigation -->\n");
    //    fprintf(index, "3 nav");
    fprintf(index, "</td></tr></table>\n");
    fprintf(index, "\n");
    fprintf(index, "</td>\n");
    fprintf(index, "<td valign='top' align='center' width='100%'>\n");
    fprintf(index, "\n");
    fprintf(index, "<table border='0' width='445' align='center' valign='top'>\n");

```

```

fprintf(index, "<tr width=\`445\`><td width=\`445\`>\n");
fprintf(index, "\n");
fprintf(index, "<table border=\`0\` width=\`100%%\` align=\`center\` valign=\`top\` cellspacing=\`0\` cellpadding=\`0\`>\n");
fprintf(index, "<tr>\n");
fprintf(index, "<td valign=\`top\`>\n");
fprintf(index, "<!-- top banner graphic/text goes here ----->\n");
fprintf(index, "<img src=\`petaflopsplanner.gif\` width=\`183\` height=\`26\` hspace=\`0\` vspace=\`4\` alt=\`Programs\`></td>\n");
fprintf(index, "\n");
fprintf(index, "<td valign=\`top\` align=\`right\`>\n");
fprintf(index, "<a href=\`http://www.sandia.gov/Main.html\`><img border=\`0\` src=\`logo.gif\` align=\`center\` width=\`151\` hspace=\`0\` height=\`60\` vspace=\`0\` alt=\`Sandia National Laboratories\`></a></td></tr>\n");
fprintf(index, "<tr><td colspan=\`2\`>\n");
fprintf(index, "<hr>\n");
fprintf(index, "</td></tr>\n");
fprintf(index, "</table>\n");
fprintf(index, "\n");
fprintf(index, "<center>\n");
fprintf(index, "\n");
fprintf(index, "<!-- body begins here ----->\n");
fprintf(index, "<table border=\`0\` width=\`100%%\` align=\`top\` cellspacing=\`0\` cellpadding=\`0\`>\n");
fprintf(index, "<tr>\n");
fprintf(index, "<td>\n");
fprintf(index, "%s\n", Out1a);
// fprintf(index, "<h2>Help</h2>\n");

fprintf(index, "Plans a parallel supercomputer with a specified performance level.<p>\n");

fprintf(index, "<h3>Technology</h3>\n");

fprintf(index, "The software plans a supercomputer based on projections of CMOS technology up to 15 years into the future.\n");
fprintf(index, "Projections are based on the <a href=http://public.itrs.net/Semiconductor Industries Association's (SIA's International Technology Roadmap for Semiconductors (ITRS)</a>, which generalizes Moore's Law to dozens of parameters projected 15 years into the future.<p>\n");

fprintf(index, "<h3>Architectures</h3>\n");

fprintf(index, "The software implements three well-known architectures:\n");
fprintf(index, "<ul>\n");
fprintf(index, "<li><img src=pimchip.gif align=right>Processor-In-Memory architecture whereby an entire node is implemented on a single chip. "
"Each chip contains one or more microprocessor cores and DRAM. "
"The cores may be conventional CISC/RISC design or multiple issues such as VLIW or Superscalar.\n");
fprintf(index, "<li><img src=redchip.gif align=right>Discrete components, as in ASCI Red. "
"Each node in this architecture is an Symmetric MultiProcessor (SMP) with one or more microprocessor chips, one of more DRAM chips, and a ASIC wormhole router chip. "
"filler filler filler filler filler\n");
fprintf(index, "<li><img src=ncube.gif align=right>Combined processor and router architecture, as in the nCUBE. "
"Each node contains one ASIC with a wormhole router and one or more CPU cores and DRAM chips.\n");
fprintf(index, "</ul>\n");

fprintf(index, "The software assumes a 3-d mesh interconnect.<p>\n");

fprintf(index, "<h3>Design Optimization</h3>\n");

fprintf(index, "The software attempts to balance the computers by five parameters:<p>\n");

fprintf(index, "<ul>\n");
fprintf(index, "<li>I/O bandwidth from each processor to its neighbor\n");
fprintf(index, "<li>Cumulative I/O bandwidth from each processor to all neighbors combined\n");
fprintf(index, "<li>Memory size\n");
fprintf(index, "<li>Main memory bus bandwidth\n");
fprintf(index, "<li>Technology derating factor\n");
fprintf(index, "</ul>\n");

fprintf(index, "<h4>Derated Flops</h4>\n");

fprintf(index, "The software uses the concept of \`derated flops\` to find the most cost effective design.\n");
fprintf(index, "Specifically, the software calculates the highest FLOP rate that could be claimed for each node while meeting all the balance requirements.\n");
fprintf(index, "The summary screen then reports the layout within each architecture providing the highest derated flops per cost.<p>\n");

fprintf(index, "Each layout page includes a navigation section to permit the user to view designs using technology of different years and with different numbers of processors per node.\n");
fprintf(index, "Each of these design will be balanced, but will generally be of higher cost than the designed optimal design.<p>\n");

fprintf(index, "<h4>Technology Derating Factor</h4>\n");

fprintf(index, "The software uses a \`technology derating factor\` which if a form of \`fudge factor.\n");
fprintf(index, "It has been known for years that the best technology goes to commercial and consumer products.\n");
fprintf(index, "Supercomputers tend to get technology a few years later, with the delay being related to the negotiating power of the Government, the public relations value of science, etc. To account for this, the software derates the performance of microprocessors and ASICs by a selectable factor (default .5).\n");
fprintf(index, "Memories are not affected.<p>\n");

fprintf(index, "<h4>Memory Size</h4>\n");

fprintf(index, "The memory size parameter is given in bytes/FLOPs at a 1 teraflops cumulative processor speed.\n");
fprintf(index, "In accordance with ASCI design rules, the parameter is multiplied by (target flops/1 teraflops)<sup>.25</sup>.\n");
fprintf(index, "(This factor is somewhat heuristic. However, the justification is based on scaling a 3-d finite difference equation by 2 in linear dimension.\n");
fprintf(index, "Such a scaling would require 2<sup>3</sup> more memory but 2<sup>4</sup> more computation because the timestep must be divided along with linear dimension.)<p>\n");

fprintf(index, "<h4>Power Consumption</h4>\n");

fprintf(index, "The software reports, but does not optimize power consumption per chip and over the whole machine.\n");
fprintf(index, "Power consumption per chip is based on equivalent real chips in 2002 scaled by CMOS power scaling rules.\n");

fprintf(index, "<h3>Output Legend</h3>\n");

fprintf(index, "<ul>\n");
fprintf(index, "<li>Squares represent integrated circuits. The size of a square represents the size of the integrated circuit die, with the scaling factor consistent across all screens.\n");
fprintf(index, "<li>Integrated circuit I/O pins are represented by horizontal bar graphs. The overall scale of the graphs is consistent across all screens.\n");
fprintf(index, "<li>Yellow represents memory. Yellow squares represent DRAM chips. Yellow regions in bar graphs represent pins devoted to the memory bus.\n");
fprintf(index, "<li>Alternating red and blue represent processors. Red and blue squares represent processor chips or cores. Red and blue regions in the bar graphs represent pins devoted to chip-to-chip interconnections.\n");
fprintf(index, "<li>Black squares represent wormhole routers.\n");
fprintf(index, "</ul>\n");

fprintf(index, "%s\n", Out2);
fprintf(index, "</td></tr>\n");

```

```

fprintf(index, "</table>\n");
fprintf(index, "</center>\n");
fprintf(index, "\n");
fprintf(index, "<!-- body ends here ----->\n");
fprintf(index, "</td></tr></table>\n");
fprintf(index, "\n");
fprintf(index, "</td></tr></table>\n");
fprintf(index, "\n");
fprintf(index, "<hr width='100%'>\n");
fprintf(index, "\n");
fprintf(index, "<table align='top' border='0' width='100%'>\n");
fprintf(index, "<tr align='center'>\n");
fprintf(index, "<td valign='top' width='140'>\n");
fprintf(index, "<table border='0' width='140'>\n");
fprintf(index, "<tr><td align='center' width='120' valign='top'>\n");
fprintf(index, "<font size='-1' color='FFFFFF'>\n");
fprintf(index, "<br></font>\n");
fprintf(index, "</td>\n");
fprintf(index, "<td width='20'>\n");
fprintf(index, "<br>\n");
fprintf(index, "</td></tr></table>\n");
fprintf(index, "\n");
fprintf(index, "</td>\n");
fprintf(index, "\n");
fprintf(index, "<td valign='top' align='center' width='100%'>\n");
fprintf(index, "\n");
fprintf(index, "<table border='0' width='100%' align='center' valign='top'>\n");
fprintf(index, "<tr valign=top><td>\n");
fprintf(index, "<font size='-1'><center>\n");
fprintf(index, "<a href='#TOP'>Back to top of page</a> || \n");
fprintf(index, "<a href='http://www.sandia.gov/feedback.htm'>Questions and Comments</a> || \n");
fprintf(index, "<a href='http://www.sandia.gov/dis.htm'>Acknowledgment and Disclaimer</a></center></font>\n");
fprintf(index, "</td></tr></table>\n");
fprintf(index, "\n");
fprintf(index, "</td></tr></table>\n");
fprintf(index, "\n");
fprintf(index, "</html>\n");
fprintf(index, "\n");

return 0;
}

void WebServe(SOCKET theClient, char *Path, Query &qx) {

char *File = Path;
if (!) for (char *x = Path; *x != 0; x++)
if (*x == '/')
File = x + 1;

// print the plain form
if (strcmp(Path, "/") == 0 || strcmp(Path, "/index.htm") == 0) {
send(theClient, "HTTP/1.0 200\r\n", 14, 0);
send(theClient, "Content-type: ", 14, 0);
send(theClient, "text/html", 9, 0);
send(theClient, "\r\n", 2, 0);
send(theClient, "\r\n", 2, 0);

FILE *index = fopen("tmp.htm", "wb");
Summary(index, qx, 0);
fclose(index);
FILE *t = fopen("tmp.htm", "rb");
char buf[1234];
int i;
do {
i = fread(buf, 1, sizeof buf, t);
if (i > 0) send(theClient, buf, i, 0);
} while (i == sizeof buf);

fclose(t);
}

// print an output table with a form at the bottom
else if (strcmp(Path, "/planner") == 0 && qx.Command == 2) {
send(theClient, "HTTP/1.0 200\r\n", 14, 0);
send(theClient, "Content-type: ", 14, 0);
send(theClient, "text/html", 9, 0);
send(theClient, "\r\n", 2, 0);
send(theClient, "\r\n", 2, 0);

FILE *index = fopen("tmp.htm", "wb");
Summary(index, qx, 1);
fclose(index);
FILE *t = fopen("tmp.htm", "rb");
char buf[1234];
int i;
do {
i = fread(buf, 1, sizeof buf, t);
if (i > 0) send(theClient, buf, i, 0);
} while (i == sizeof buf);

fclose(t);
}

// print help
else if (strcmp(Path, "/help.htm") == 0) {
send(theClient, "HTTP/1.0 200\r\n", 14, 0);
send(theClient, "Content-type: ", 14, 0);
send(theClient, "text/html", 9, 0);
send(theClient, "\r\n", 2, 0);
send(theClient, "\r\n", 2, 0);

FILE *index = fopen("tmp.htm", "wb");
Help(index);
fclose(index);
FILE *t = fopen("tmp.htm", "rb");
char buf[1234];
int i;
do {
i = fread(buf, 1, sizeof buf, t);
if (i > 0) send(theClient, buf, i, 0);
} while (i == sizeof buf);

fclose(t);
}

```



```
28, 250, 241, 39, 80, 150, 36, 117, 146, 60, 32, 148, 168, 76, 163, 17, 121, 58, 157, 10, 82, 224, 129, 171, 88, 11, 74, 93, 216, 148, 98, 206,
174, 84, 77, 46, 197, 202, 52, 228, 214, 176, 97, 193, 6, 77, 186, 246, 232, 201, 182, 46, 127, 242, 20, 153, 208, 37, 220, 155, 53, 143, 114,
101, 91, 23, 99, 74, 140, 53, 95, 218, 133, 43, 88, 111, 222, 190, 6, 227, 242, 173, 89, 22, 170, 99, 179, 133, 51, 70, 140, 57, 89, 50, 98,
148, 123, 163, 222, 181, 11, 19, 48, 220, 198, 131, 223, 110, 38, 9, 246, 177, 105, 185, 163, 57, 159, 246, 204, 88, 225, 73, 208, 128, 141,
166, 22, 105, 115, 54, 108, 168, 89, 73, 235, 182, 122, 85, 43, 76, 208, 176, 115, 3, 213, 42, 156, 120, 110, 172, 151, 87, 23, 71, 105, 220,
244, 119, 219, 237, 217, 35, 3, 247, 238, 151, 61, 243, 174, 229, 225, 251, 125, 128, 28, 189, 213, 212, 227, 243, 166, 175, 108, 248, 97, 249,
248, 248, 125, 38, 159, 85, 3, 106, 149, 220, 126, 179, 241, 102, 222, 78, 153, 113, 87, 82, 120, 7, 222, 23, 33, 93, 85, 153, 101, 93, 105,
206, 73, 168, 94, 129, 213, 145, 167, 32, 89, 127, 61, 22, 162, 89, 219, 105, 230, 161, 129, 151, 45, 136, 87, 138, 32, 230, 87, 162, 95, 5, 2,
55, 97, 121, 39, 158, 197, 31, 131, 196, 125, 135, 25, 132, 250, 105, 168, 30, 125, 148, 213, 232, 21, 119, 221, 233, 56, 151, 131, 51, 162,
150, 226, 68, 211, 129, 104, 228, 133, 72, 242, 120, 163, 84, 77, 81, 55, 216, 143, 76, 182, 247, 32, 146, 246, 97, 214, 99, 119, 45, 202, 184,
164, 127, 139, 165, 216, 148, 145, 2, 246, 167, 227, 138, 40, 138, 23, 227, 144, 38, 166, 233, 35, 154, 95, 218, 136, 161, 143, 13, 246, 181,
33, 91, 25, 238, 72, 100, 94, 183, 49, 86, 150, 144, 173, 101, 105, 98, 159, 71, 18, 184, 152, 142, 122, 126, 70, 40, 153, 171, 145, 152, 212,
139, 237, 67, 74, 220, 152, 144, 198, 183, 40, 151, 123, 226, 246,
104, 166, 81, 169, 184, 155, 140, 66, 189, 182, 165, 162, 57, 50, 136, 105, 133, 230, 53, 38, 102, 167, 113, 94, 254, 184, 211,
157, 177, 78, 116, 91, 125, 59, 45, 120, 106, 172, 193, 141, 247, 98, 125, 173, 6, 232, 168, 161, 126, 46, 197, 35, 157, 88, 222, 106, 101,
173, 7, 145, 213, 81, 139, 10, 133, 9, 108, 152, 205, 214, 135, 16, 136, 99, 58, 27, 45, 180, 14, 105, 107, 235, 180, 224, 98, 43, 30, 114,
222, 86, 27, 32, 183, 244, 89, 139, 214, 186, 74, 225, 201, 238, 187, 240, 198, 43, 111, 166, 54, 206, 107, 239, 189, 248, 206, 164, 86, 190,
252, 246, 235, 111, 131, 245, 254, 43, 240, 192, 242, 150, 75, 240, 193, 19, 5, 4, 0, 59, };
```

```
BigGIFHelper(theClient, petaflopsplanner, 1418);
```

```
}
else if (strcmp(File, "logo.gif") == 0) {
    static unsigned char logo[1780] = { 71, 73, 70, 56, 57, 97, 151, 0, 60, 0, 179, 255, 0, 192, 192, 192, 204, 255, 255, 204, 204, 255,
204, 204, 204, 153, 204, 255, 153, 204, 204, 153, 153, 153, 102, 204, 204, 102, 102, 153, 204, 102, 102, 102, 51, 153, 204, 51, 51, 51, 0, 153, 204,
0, 0, 0, 0, 0, 0, 0, 33, 249, 4, 1, 0, 0, 0, 44, 0, 0, 0, 0, 151, 0, 60, 0, 0, 4, 255, 16, 200, 73, 171, 189, 56, 235, 205, 187, 255,
96, 248, 5, 129, 96, 18, 104, 170, 174, 132, 41, 144, 129, 40, 207, 16, 13, 18, 197, 129, 32, 74, 239, 255, 152, 160, 240, 183, 67, 28, 10,
219, 217, 96, 105, 107, 58, 55, 1, 222, 112, 74, 173, 246, 24, 10, 66, 104, 144, 104, 120, 19, 3, 219, 192, 96, 0, 112, 203, 79, 27, 193, 202,
110, 11, 17, 73, 206, 192, 219, 88, 208, 195, 52, 131, 23, 160, 95, 164, 107, 5, 110, 130, 131, 10, 113, 26, 122, 13, 97, 115, 13, 104, 51,
139, 102, 11, 9, 127, 51, 107, 132, 150, 86, 8, 29, 93, 126, 18, 118, 146, 52, 143, 147, 52, 1, 152, 70, 71, 5, 168, 44, 44, 168, 168, 7, 58,
82, 84, 5, 28, 155, 19, 6, 9, 104, 182, 9, 96, 18, 100, 185, 187, 188, 186, 136, 102, 183, 192, 186, 120, 162, 24, 129, 66, 5, 47, 162, 36, 4,
7, 67, 179, 94, 199,
181, 116, 117, 157, 215, 117, 97, 93, 218, 124, 216, 221, 119, 200, 24, 66, 7, 227, 22, 149, 64, 90, 26, 139, 11, 6, 213, 158,
3, 158, 0, 118, 11, 99, 94, 239, 248, 92, 123, 125, 139, 239, 180, 231, 40, 164, 243, 177, 46, 3, 9, 23, 170, 76, 24, 218, 0, 171, 71, 166, 13,
136, 240, 73, 144, 103, 239, 155, 159, 121, 0, 186, 220, 194, 246, 173, 129, 69, 138, 97, 255, 16, 85, 59, 23, 13, 8, 20, 54, 14, 100, 121, 24,
216, 163, 131, 60, 58, 159, 40, 244, 161, 215, 224, 147, 198, 153, 29, 45, 86, 16, 25, 112, 66, 67, 5, 230, 52, 144, 98, 163, 178, 195, 208, 24,
31, 2, 60, 236, 99, 52, 204, 142, 151, 139, 53, 37, 220, 228, 40, 108, 38, 23, 167, 212, 122, 74, 8, 82, 20, 131, 128, 54, 39, 57, 4, 73, 250,
161, 94, 198, 47, 180, 48, 78, 229, 84, 21, 155, 83, 93, 89, 181, 6, 41, 232, 21, 44, 136, 185, 25, 94, 54, 66, 196, 115, 166, 218, 154, 56,
219, 218, 203, 202, 179, 231, 81, 31, 100, 13, 146, 0, 240, 117, 74, 80, 15, 63, 195, 82, 88, 20, 179, 79, 96, 183, 81, 207, 110, 100, 203,
175, 142, 176, 142, 35, 145, 29, 238, 177, 80, 67, 227, 33, 143, 59, 148, 244, 33, 153, 130, 217, 108, 238, 56, 154, 253, 187, 49, 81, 78, 203,
89, 187, 133, 118, 22,
164, 116, 134, 211, 111, 64, 172, 238, 145, 218, 2, 162, 72, 78, 203, 212, 115, 10, 213, 102, 212, 122, 9, 156, 126, 124, 138,
117, 247, 164, 209, 10, 54, 0, 15, 242, 208, 131, 50, 31, 221, 49, 24, 192, 202, 180, 163, 187, 5, 126, 186, 160, 209, 8, 9, 21, 122, 157, 199,
199, 87, 52, 28, 68, 160, 42, 21, 195, 133, 220, 87, 17, 231, 187, 67, 15, 239, 84, 192, 196, 255, 7, 214, 77, 84, 224, 56, 163, 133, 119,
137, 27, 12, 20, 196, 82, 120, 90, 69, 8, 66, 130, 20, 44, 232, 134, 131, 64, 40, 225, 134, 39, 17, 81, 161, 133, 68, 77, 176, 93, 118, 24,
112, 97, 204, 68, 39, 106, 242, 75, 19, 41, 58, 49, 218, 99, 216, 129, 184, 140, 136, 245, 149, 8, 211, 68, 113, 109, 224, 143, 19, 59, 62,
241, 226, 4, 49, 202, 8, 68, 81, 35, 230, 69, 7, 39, 139, 20, 120, 6, 36, 243, 137, 33, 145, 143, 64, 100, 21, 68, 214, 100, 192, 34,
18, 37, 153, 129, 29, 141, 164, 209, 163, 139, 81, 2, 57, 101, 44, 52, 154, 100, 99, 29, 81, 105, 105, 6, 25, 120, 232, 165, 72, 53, 75, 28,
195, 4, 155, 147, 145, 49, 193, 151, 77, 252, 40, 65, 144, 99, 2, 37, 166, 153, 87, 226, 179, 135, 150, 228, 129, 161, 77, 95, 215, 124, 242,
212, 141, 47, 49, 250, 36,
152, 63, 60, 54, 34, 105, 48, 252, 52, 23, 12, 254, 249, 32, 37, 160, 22, 36, 169, 15, 53, 34, 185, 233, 73, 62, 137, 248, 163,
23, 0, 79, 129, 182, 201, 61, 165, 62, 154, 103, 152, 158, 18, 76, 26, 158, 165, 64, 36, 198, 18, 113, 127, 254, 96, 100, 34, 241, 128, 202, 17,
123, 92, 154, 225, 43, 103, 80, 161, 129, 143, 122, 194, 50, 229, 170, 13, 122, 50, 22, 156, 255, 79, 85, 216, 90, 78, 174, 62, 236, 186, 143,
161, 182, 81, 0, 44, 83, 73, 178, 167, 83, 176, 168, 150, 135, 163, 178, 226, 190, 26, 41, 181, 224, 81, 64, 43, 82, 19, 220, 234, 231, 158,
86, 118, 58, 172, 150, 87, 221, 24, 108, 183, 153, 249, 85, 94, 150, 209, 209, 81, 198, 178, 53, 52, 27, 227, 172, 85, 20, 52, 233, 166, 186,
158, 185, 132, 160, 173, 122, 54, 207, 189, 212, 200, 171, 175, 177, 140, 32, 2, 23, 185, 93, 50, 11, 43, 0, 3, 127, 72, 133, 193, 51, 194,
203, 169, 128, 89, 121, 50, 44, 47, 207, 113, 27, 113, 190, 152, 81, 60, 94, 121, 193, 2, 60, 202, 198, 216, 49, 160, 96, 193, 34, 98, 49, 100,
153, 9, 7, 106, 91, 56, 137, 120, 187, 109, 25, 73, 234, 241, 201, 196, 18, 184, 167, 50, 198, 105, 8, 28, 101, 1, 116, 89, 81, 80, 0, 168,
236, 28, 107, 188, 36, 219, 134, 101,
34, 70, 103, 35, 9, 196, 92, 83, 149, 178, 203, 96, 255, 91, 174, 198, 231, 138, 76, 144, 5, 82, 179, 253, 67, 149, 35, 79, 22,
87, 117, 22, 51, 119, 150, 59, 161, 126, 193, 23, 77, 46, 111, 210, 47, 211, 80, 166, 189, 213, 15, 116, 13, 78, 102, 5, 86, 9, 21, 247, 157,
232, 225, 33, 95, 69, 221, 232, 18, 73, 83, 140, 52, 222, 158, 103, 217, 160, 193, 229, 255, 82, 209, 185, 67, 79, 147, 230, 166, 59, 129, 58,
21, 240, 201, 154, 219, 107, 95, 189, 56, 129, 7, 118, 218, 250, 157, 175, 163, 45, 186, 225, 61, 132, 101, 122, 237, 168, 247, 128, 225, 234,
28, 246, 78, 1, 133, 208, 158, 254, 187, 21, 182, 215, 218, 110, 134, 190, 39, 143, 1, 118, 234, 190, 93, 58, 241, 207, 179, 43, 65, 166, 26,
78, 246, 122, 156, 202, 195, 30, 2, 243, 62, 233, 252, 46, 186, 211, 82, 0, 28, 3, 137, 101, 90, 156, 220, 103, 91, 224, 173, 242, 56, 141,
208, 219, 4, 254, 21, 119, 251, 247, 170, 43, 176, 67, 28, 249, 157, 127, 167, 204, 118, 102, 150, 134, 46, 31, 104, 159, 7, 176, 227, 155,
197, 12, 175, 10, 231, 243, 13, 0, 34, 179, 171, 140, 169, 207, 127, 78, 232, 26, 235, 182, 55, 22, 15, 76, 106, 99, 28, 96, 224, 153, 50, 54,
134, 70, 176, 103, 64, 119, 10, 144, 129, 222,
180, 38, 17, 238, 163, 73, 99, 144, 19, 19, 72, 56, 17, 17, 214, 194, 133, 0, 192, 75, 7, 46, 40, 56, 177, 144, 110, 131, 140,
59, 18, 55, 234, 240, 150, 9, 132, 3, 114, 53, 233, 2, 171, 62, 117, 141, 48, 96, 165, 34, 70, 139, 142, 85, 176, 178, 139, 70, 109, 67, 2, 26,
228, 0, 13, 53, 192, 10, 226, 208, 107, 39, 60, 11, 96, 130, 101, 25, 145, 255, 68, 164, 54, 100, 224, 146, 45, 48, 119, 20, 90, 68, 132,
12, 152, 185, 197, 170, 196, 136, 145, 159, 84, 239, 2, 2, 240, 158, 16, 108, 102, 193, 247, 93, 113, 71, 69, 19, 91, 122, 202, 163, 30, 158,
0, 132, 61, 93, 163, 151, 175, 152, 210, 143, 172, 248, 99, 15, 119, 155, 158, 29, 161, 224, 138, 34, 56, 178, 145, 173, 185, 64, 166, 72, 116,
69, 51, 180, 201, 87, 71, 107, 153, 84, 0, 195, 17, 236, 105, 230, 27, 146, 80, 147, 29, 238, 65, 44, 65, 50, 34, 75, 34, 68, 209, 27, 199,
113, 43, 253, 237, 175, 92, 78, 12, 27, 177, 248, 182, 201, 205, 104, 139, 137, 160, 76, 22, 30, 70, 121, 153, 216, 4, 81, 55, 17, 25, 201, 27,
20, 56, 137, 73, 102, 129, 29, 143, 138, 136, 83, 72, 137, 178, 98, 213, 18, 39, 141, 234, 97, 32, 231, 86, 49, 61, 70, 164, 136, 29, 201, 150,
4, 220, 101, 63,
87, 164, 162, 5, 47, 128, 1, 20, 96, 112, 2, 28, 228, 96, 93, 171, 28, 23, 26, 240, 120, 178, 111, 241, 145, 147, 156, 88, 213,
39, 167, 153, 45, 94, 234, 209, 84, 158, 28, 198, 163, 230, 215, 167, 42, 164, 68, 71, 79, 50, 233, 76, 205, 224, 68, 104, 81,
161, 231, 46, 101, 217, 70, 53, 177, 201, 78, 52, 225, 196, 54, 251, 185, 32, 87, 162, 111, 164, 157, 132, 105, 103, 215, 144, 117, 22, 52,
198, 51, 51, 243, 144, 160, 33, 5, 186, 141, 140, 214, 228, 87, 28, 1, 31, 69, 253, 25, 201, 172, 193, 4, 58, 119, 232, 134, 47, 203, 192, 23,
96, 162, 180, 38, 120, 252, 194, 9, 95, 230, 135, 94, 210, 228, 22, 245, 160, 204, 203, 98, 194, 179, 149, 90, 193, 162, 46, 197, 135, 50, 87,
134, 158, 84, 101, 195, 95, 58, 185, 28, 154, 62, 177, 76, 154, 64, 213, 167, 78, 68, 226, 53, 64, 39, 144, 117, 25, 85, 1, 72, 0, 65, 156,
176, 151, 66, 75, 154, 245, 172, 33, 52, 33, 8, 215, 52, 86, 237, 181, 16, 132, 112, 149, 19, 12, 151, 0, 195, 229, 9, 0, 7, 175, 152, 210, 14,
78, 65, 0, 98, 102, 239, 175, 51, 128, 65, 9, 92, 64, 216, 194, 134, 211, 128, 128, 77, 108, 7, 34, 0, 0, 59, };
```

```
BigGIFHelper(theClient, logo, 1780);
```

```
}
else if (strcmp(File, "pimchip.gif") == 0) {
    static unsigned char pimchip[1277] = { 71, 73, 70, 56, 55, 97, 83, 0, 54, 0, 247, 0, 0, 0, 0, 128, 0, 0, 0, 128, 0, 128, 128, 0, 0,
0, 128, 128, 0, 128, 0, 128, 128, 192, 192, 192, 192, 220, 192, 166, 202, 240, 0, 0, 0, 0, 0, 42, 0, 0, 85, 0, 0, 127, 0, 0, 170, 0, 0, 212, 0,
42, 0, 0, 42, 42, 0, 42, 85, 0, 42, 127, 0, 42, 170, 0, 42, 212, 0, 85, 0, 0, 85, 42, 0, 85, 127, 0, 85, 170, 0, 85, 210, 0, 127, 0,
0, 127, 42, 0, 127, 85, 0, 127, 127, 0, 127, 170, 0, 127, 212, 0, 170, 0, 0, 170, 42, 0, 170, 85, 0, 170, 127, 0, 170, 170, 0, 170, 212, 0,
212, 0, 0, 212, 42, 0, 212, 85, 0, 212, 127, 0, 212, 170, 0, 212, 212, 42, 0, 0, 42, 0, 42, 42, 0, 85, 42, 0, 127, 42, 0, 170, 42, 0, 212, 42,
42, 0, 42, 42, 42, 42, 85, 42, 42, 127, 42, 42, 170, 42, 42, 212, 42, 85, 0, 42, 85, 42, 42, 85, 85, 42, 85, 127, 42, 85, 170, 42, 85, 212,
42, 127, 0, 42, 127, 42, 42, 127, 85, 42, 127, 127, 42, 127, 170, 42, 127, 212, 42, 170, 42, 0, 42, 170, 42, 42, 170, 85, 42, 170, 127, 42, 170,
170, 42, 170, 212, 42, 212, 0, 42, 212, 42, 42, 212, 85, 42, 212, 127, 42, 212, 170,
127, 85, 42, 170, 85, 42, 212, 85, 0, 85, 0, 42, 85, 0, 85, 85, 0, 170, 85, 0, 212, 85, 42, 0, 85, 42, 42, 85, 42, 85, 42, 85, 127, 85,
85, 127, 127, 85, 127, 170, 85, 127, 212, 85, 170, 0, 85, 170, 42, 85, 170, 85, 170, 170, 85, 170, 212, 85, 212, 0, 85, 212,
42, 85, 212, 85, 212, 127, 85, 212, 170, 85, 212, 170, 85, 212, 127, 0, 0, 127, 0, 85, 127, 0, 127, 127, 0, 170, 127, 0, 212, 127, 42,
0, 127, 42, 42, 127, 42, 0, 127, 127, 42, 127, 127, 85, 127, 127, 127, 170, 127, 127, 212, 127, 170, 0, 127, 170, 42, 127, 170, 85, 127,
170, 127, 127, 170, 170, 127, 170, 212, 127, 212, 0, 127, 212, 42, 127, 212, 85, 127, 212, 170, 127, 212, 170, 127, 212, 170, 0, 0, 170,
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```

        fclose (otest);
    }

    #if __GNUC__ != 0
        int rc;
    #else
        WSADATA wdata;
        int rc = WSASStartup(MAKEWORD(1,1), &wdata);
        if (rc) {
            printf("WSASStartup failed: error code = %d\n", rc);
            return 1;
        }
    #endif

    int Local_Address_Family = AF_INET;
    int Socket_Type = SOCK_STREAM;
    #if __GNUC__ != 0
        int Protocol = 0;
    #else
        int Protocol = IPPROTO_TCP;
    #endif
    u_int s = socket(Local_Address_Family, Socket_Type, Protocol);

    if (s == (u_int)INVALID_SOCKET) {
        printf("Socket call failed\n");
        return 1;
    }

    int yes = 1;
    setsockopt(s, SOL_SOCKET, SO_REUSEADDR, (const char *)&yes, sizeof(int));

    #if __GNUC__ != 0
        #define SOCKADDR_IN sockaddr_in
    #endif
    SOCKADDR_IN addr;
    addr.sin_family = Local_Address_Family;
    addr.sin_addr.s_addr = INADDR_ANY;
    #if __GNUC__ != 0
        addr.sin_port = htons(1710);
    #else
        addr.sin_port = htons(80);
    #endif

    rc = bind(s, (const struct sockaddr *) &addr, sizeof(SOCKADDR_IN));

    if (rc == SOCKET_ERROR) {
        printf("Error at bind()\n");
        return 1;
    }

    rc = listen(s, 10); // 10 is the number of clients that can be queued
    if (rc == SOCKET_ERROR) {
        printf("Error at listen()\n");
        return 0;
    }

    for (int i = 0; i < 200000; i++) {
        SOCKET theClient = accept(s, NULL, NULL);
        if (theClient == INVALID_SOCKET) {
            printf("Error at accept()\n");
            return 0;
        }

        int total = 0;
        char *p, buf[10000];
        do {
            rc = recv(theClient, buf, sizeof buf, 0);
            if (rc < 0)
                break;
            p = (char *) (total == 0 ? malloc(rc + 1) : realloc(p, total + rc + 1));
            memcpy(p + total, buf, rc);
            total += rc;
            p[total] = 0;
        } while (rc == sizeof buf);

        // printf("%s", p);

        if (p[0] == 'G' && p[1] == 'E' && p[2] == 'T' && p[3] == ' ') {
            char *q = p + 4, *e = q;
            while (*e != 0 && *e != ' ' && *e != '?')
                e++;

            char *file = (char *) malloc(e - q + 1);
            strncpy(file, q, e - q);
            file[e - q] = 0;
            // printf("file %s\n", file);

            int argc = 0;
            char **name = NULL;
            char **value = NULL;

            while (*e == '?' || *e == '&') {
                q = ++e;
                while (*e != 0 && *e != '&' && *e != '=' && *e != ' ' && *e != '\r' && *e != '\n')
                    e++;
                if (e != q) {
                    name = (char **) (argc++ == 0 ? malloc(sizeof(char *) * argc) : realloc(name,
sizeof(char *) * argc));
                    name[argc - 1] = (char *) malloc(e - q + 1);
                    strncpy(name[argc - 1], q, e - q);
                    name[argc - 1][e - q] = 0;
                    // printf("%s", name[argc - 1]);
                    if (*e == '=') {
                        q = ++e;
                        while (*e != 0 && *e != '&' && *e != ' ' && *e != '\r' && *e != '\n')
                            e++;
                    }
                } else
                    e = q;
                value = (char **) (argc == 1 ? malloc(sizeof(char *) * argc) : realloc(value,
sizeof(char *) * argc));
                value[argc - 1] = (char *) malloc(e - q + 1);
                strncpy(value[argc - 1], q, e - q);
                value[argc - 1][e - q] = 0;
            }
        }
    }

```

```

        // printf("=%s\n", value[argc - 1]);
    }
}

Query qx(argc, name, value);
WebServe(theClient, file, qx);

if (argc > 0) {
    while (argc > 0) {
        free(name[argc - 1]);
        free(value[argc-- - 1]);
    }
    free(name);
    free(value);
}
free(file);
}

free(p);

#if __GNUC__ != 0
    close(theClient);
#else
    closesocket(theClient);
#endif
}

#if __GNUC__ != 0
    close(s);
#else
    closesocket(s);
    WSACleanup();
#endif
return 0;
}

```