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Quantum Dot Cellular Automata (QDCA) Strategic Partnership: Extending Moore's Law: Part 2, Computer Sciences Issues

Erik DeBenedictis[1] (PI), Jerry Floro[1,3], Robert Hull[3], Peter Kogge[2], Craig Lent[2], Sarah Murphy[1,2], Mike Niemier[2], Marco Ottavi[1], Aaron Prager[1,2], Greg Snider[2]
([1]Sandia, [2]Notre Dame, [3]U. Virginia)

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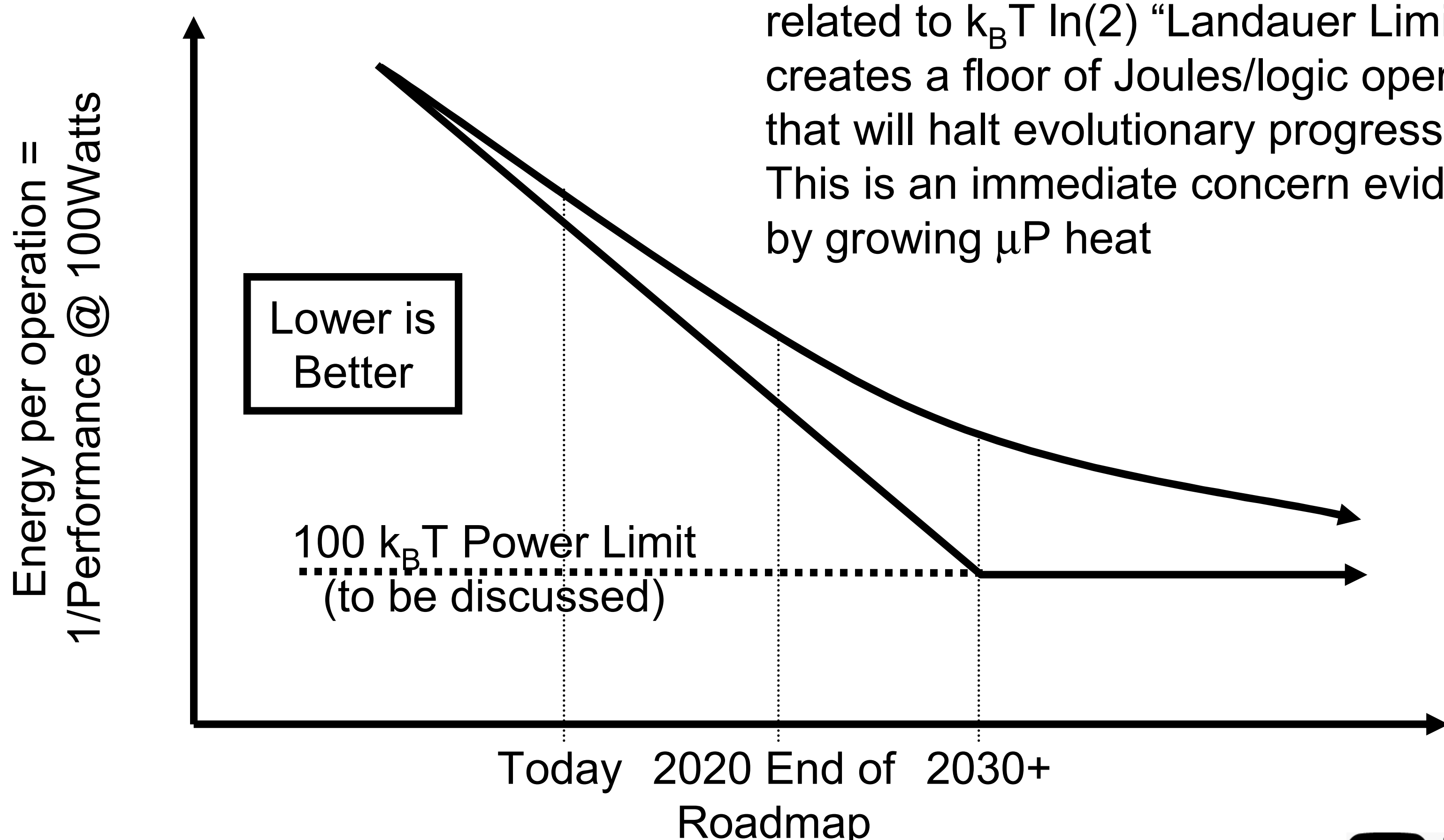
Moore's Law for Logic Switching Power

A 100 $k_B T$ "thermal device limit" closely related to $k_B T$ ln(2) "Landauer Limit" creates a floor of Joules/logic operation that will halt evolutionary progress
This is an immediate concern evidenced by growing μP heat



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Emerging Research Devices (notes 2005)

- Table shows drop in replacements for CMOS transistors that defeat limit in previous slide
- Color code: OK, marginal, unacceptable
- CNFET on table only for political reasons

> 20	>16 - 18
>18 - 20	< 16

For each Technology Entry (e.g. 1D Structures, sum horizontally over the 8 Criteria
Max Sum = 24
Min Sum = 8

Evaluation of Emerging Research Logic Device Technologies against Technology Evaluation Criteria

Logic Device Technologies	Scalability	Perform-ance	Energy Efficiency	Gain	Operational Reliability	Room Temp. Operation ***	CMOS Compatibility **	CMOS Architectural Compatibility *
1D Structures	2.4	2.4	2.1	2.4	2.3	2.9	2.4	2.6
Resonant Tunneling Devices	1.4	2.0	1.9	1.7	1.7	2.9	2.1	2.1
SETs	1.9	1.0	2.5	1.3	1.2	1.9	2.4	2.0
Molecular Devices	1.9	1.1	2.0	1.1	1.3	2.6	1.9	1.6
Ferromagnetic Devices	1.5	1.2	1.8	1.5	1.8	2.2	1.5	1.8
Spin Transistor	1.7	1.7	2.2	1.5	2.0	2.2	1.7	1.8

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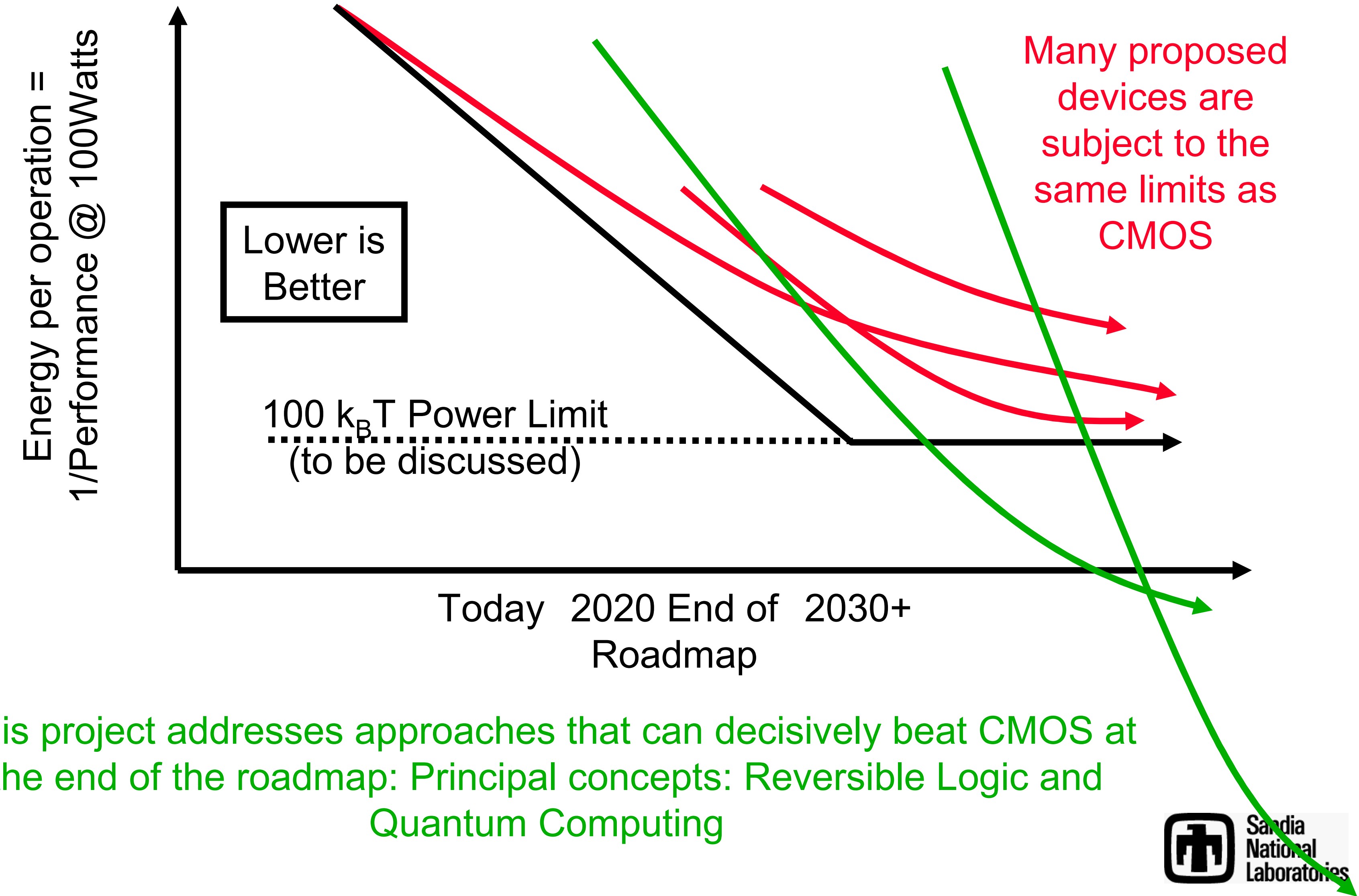
Obeying Moore's Law and Beating CMOS



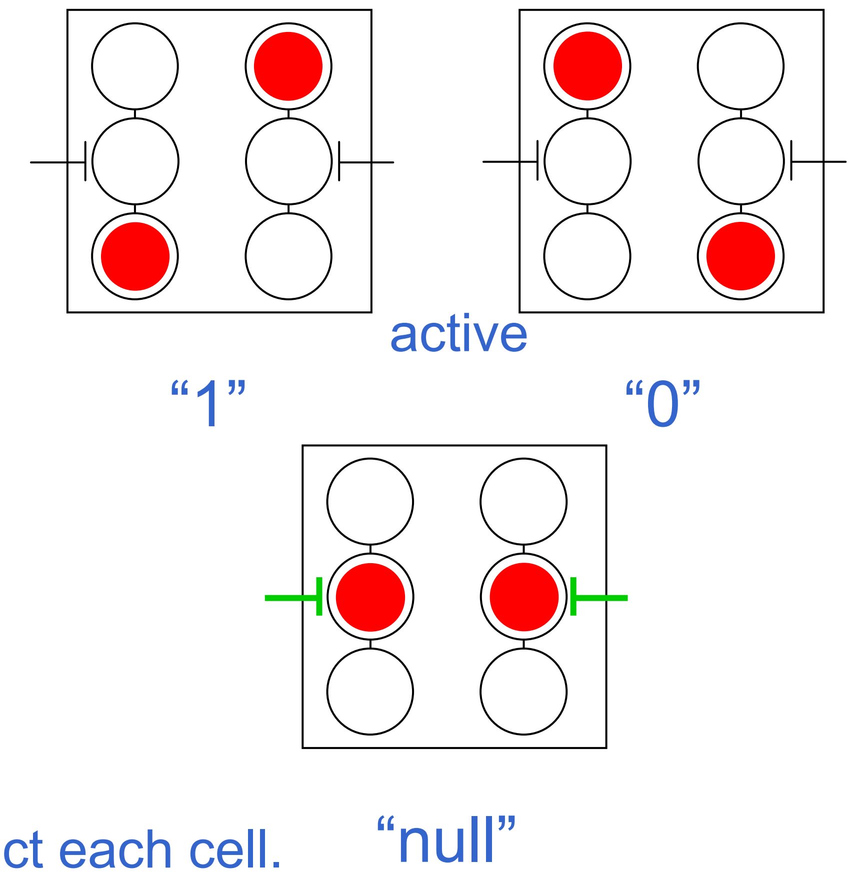
This project addresses approaches that can decisively beat CMOS at the end of the roadmap: Principal concepts: Reversible Logic and Quantum Computing

Tie Between Information and Device Physics

- We use Boolean logic today, based on AND-OR-NOT
- AND and OR gates “destroy” information, which creates heat irrespective of physical implementation (to be described later)
- This limit can be circumvented by a different form of logic that does not “destroy” information
- However, this will also require different devices…

Quantum-dot cellular automata

Represent binary information by charge configuration of cell.



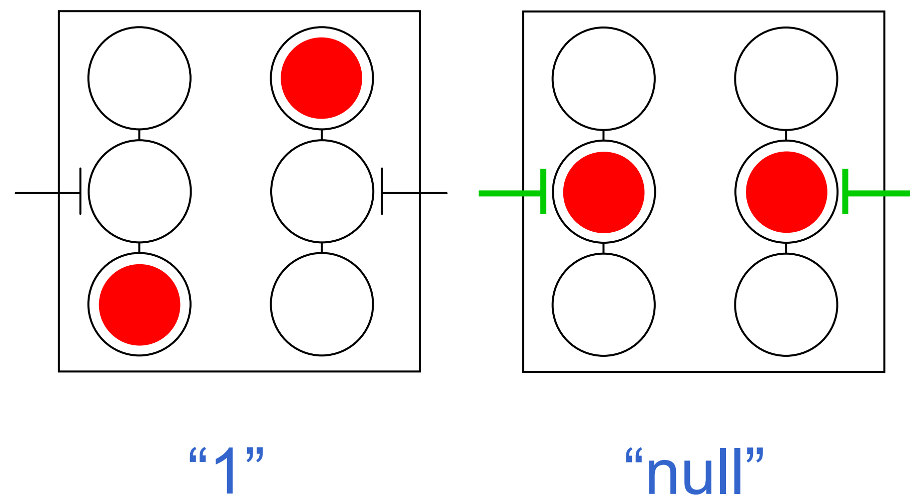
<u>QCA cell</u>

- Dots localize charge
- Two mobile charges
- Tunneling between dots
- Clock signal varies relative energies of “active” and “null” dots

Clock need not separately contact each cell.

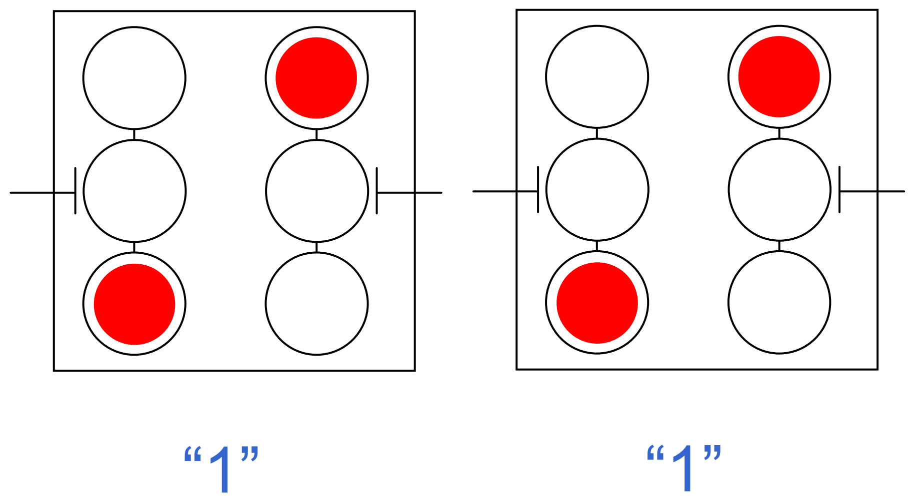
Quantum-dot cellular automata

Neighboring cells tend to align in the same state.



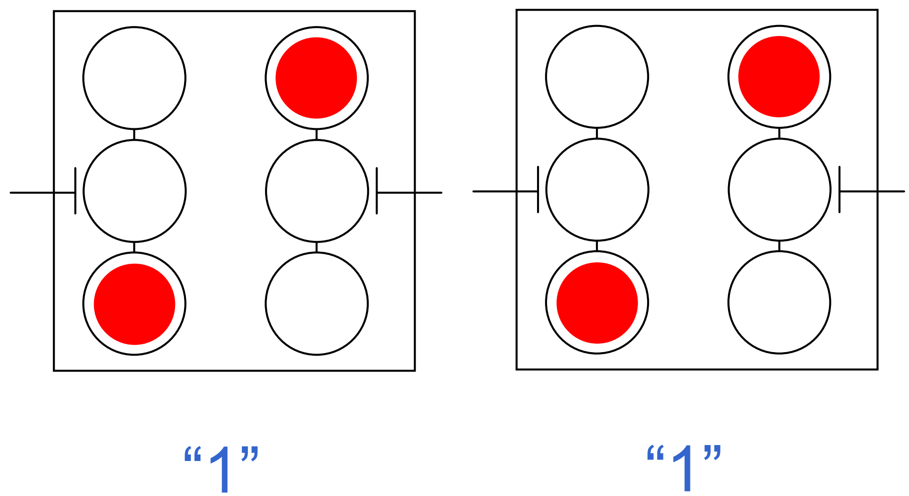
Quantum-dot cellular automata

Neighboring cells tend to align in the same state.



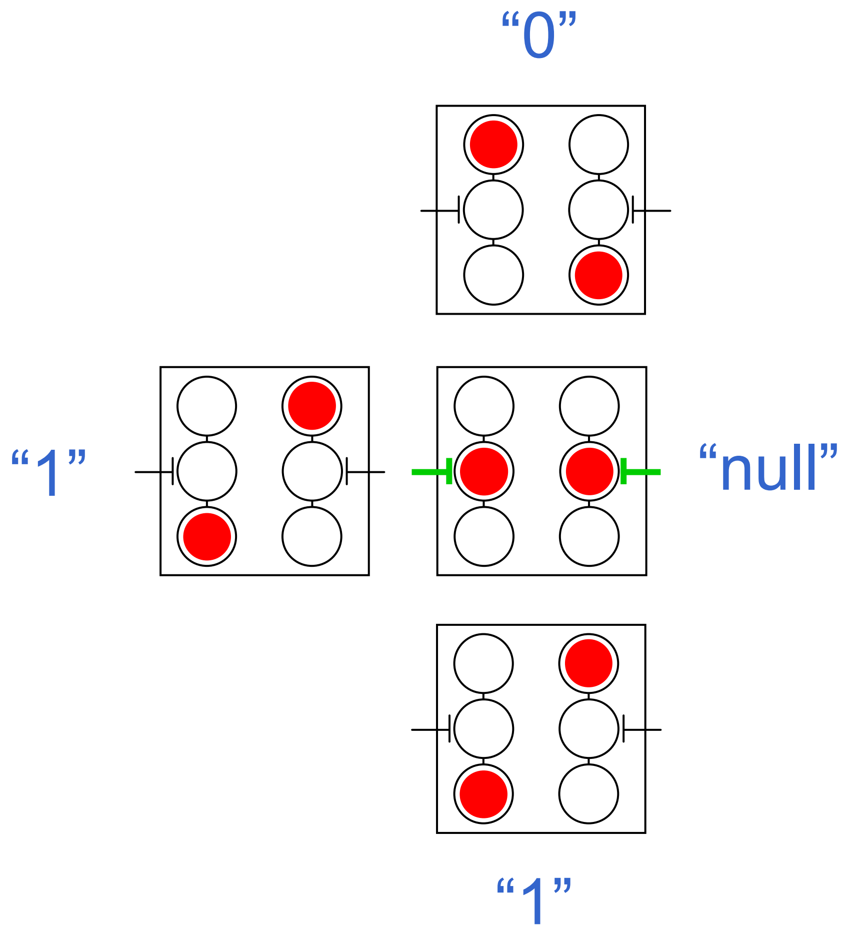
Quantum-dot cellular automata

Neighboring cells tend to align in the same state.

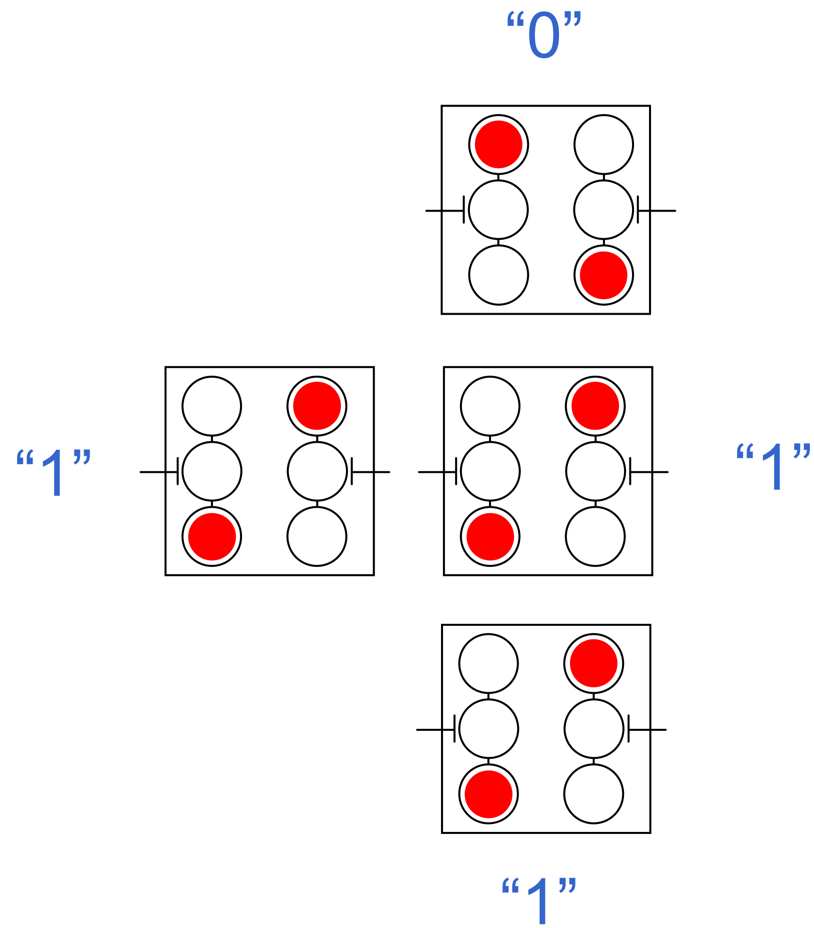


This is the COPY operation.

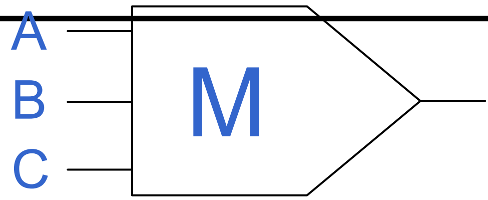
Majority Gate



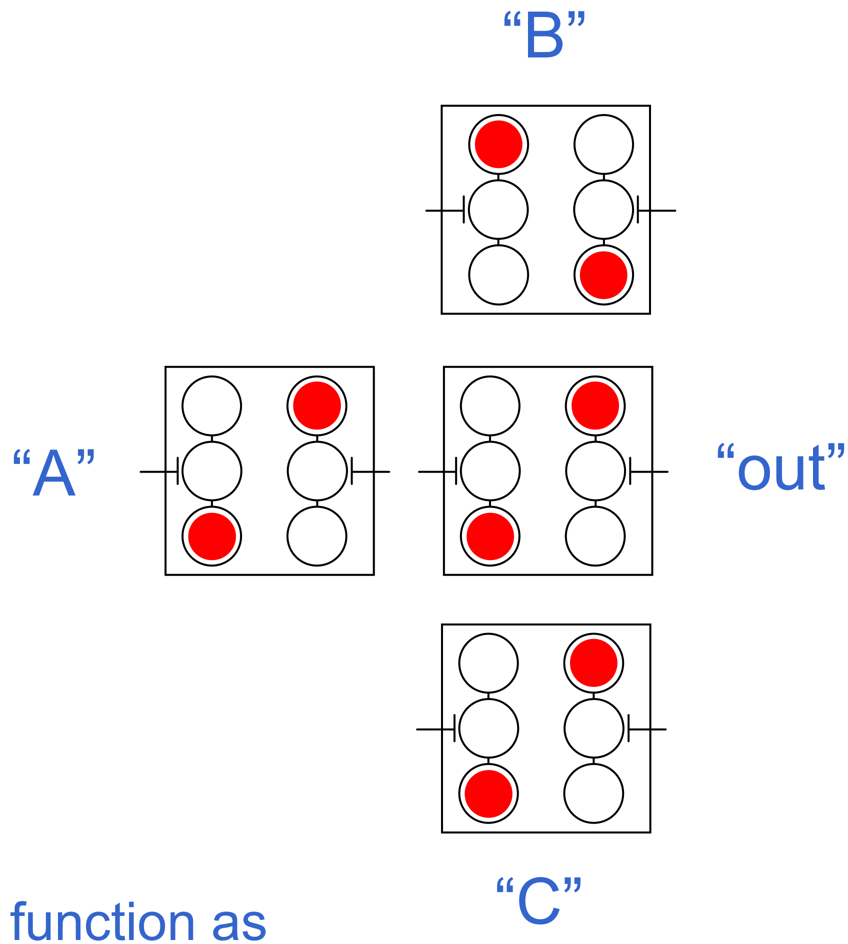
Majority Gate



Majority Gate

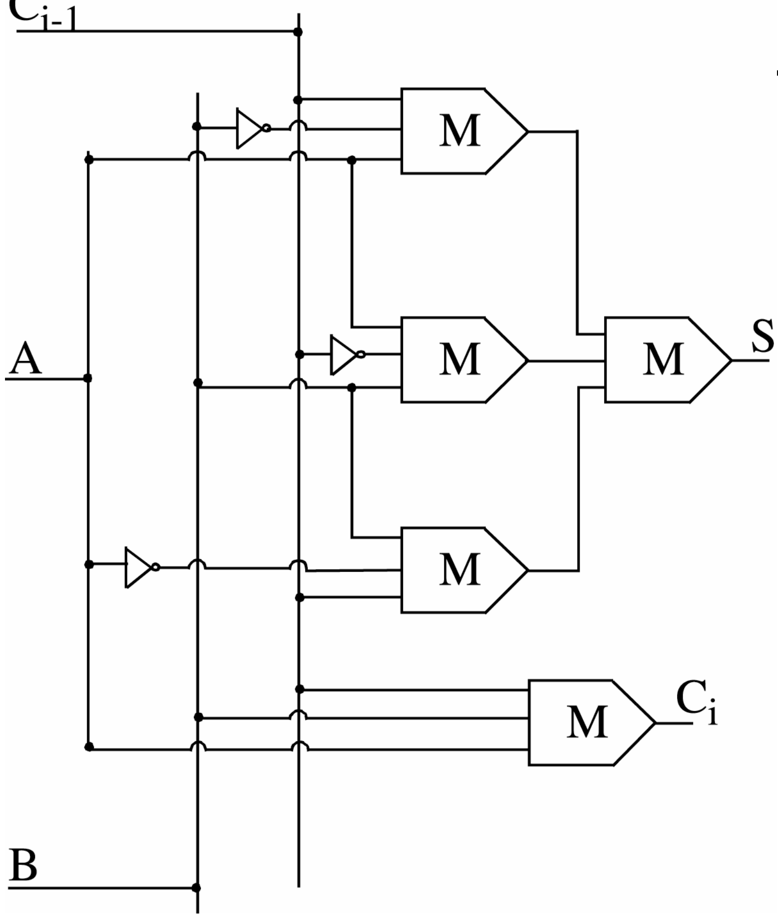


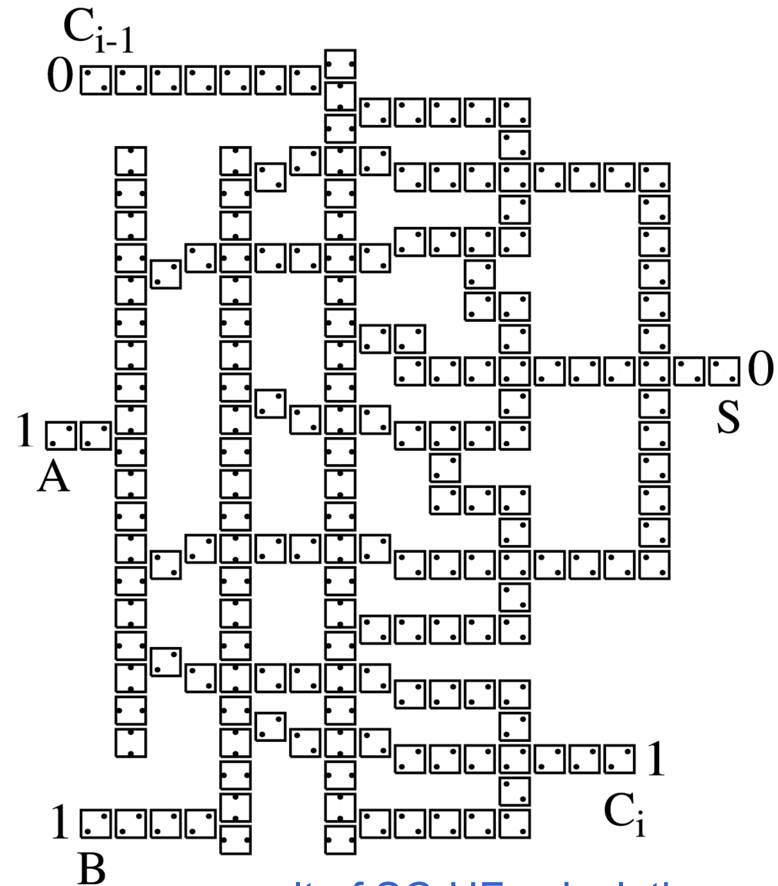
	A	B	C	Output
AND gate	0	0	0	0
	0	0	1	0
	0	1	1	1
	0	1	0	0
OR gate	1	1	0	1
	1	1	1	1
	1	0	1	1
	1	0	0	0



Three input majority gate can function as programmable 2-input AND/OR gate.

QCA single-bit full adder





result of SC-HF calculation
with site model

Hierarchical layout and design are possible.
Simple-12 microprocessor (Kogge & Niemier)

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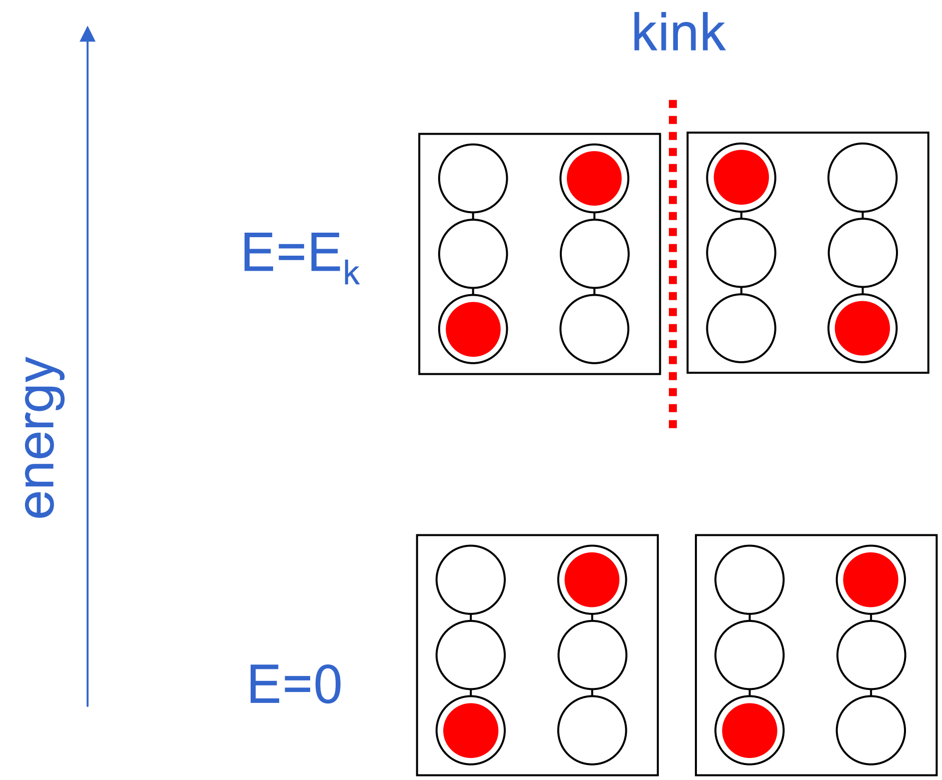
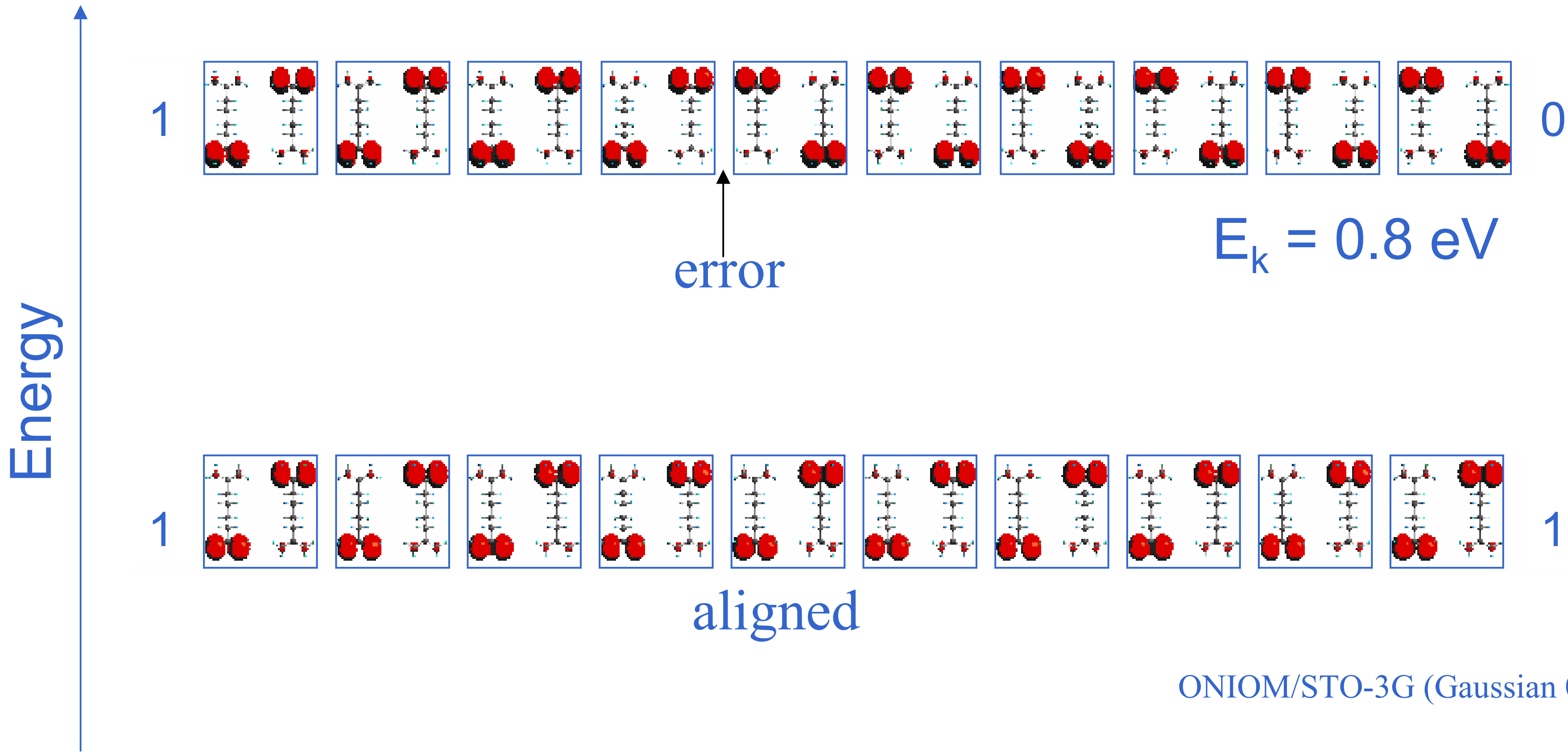
Computational wave: adder back-end

Characteristic energy



We would like "kink energy" $E_k > k_B T$.

Molecular Wire



ONIOM/STO-3G (Gaussian 03)

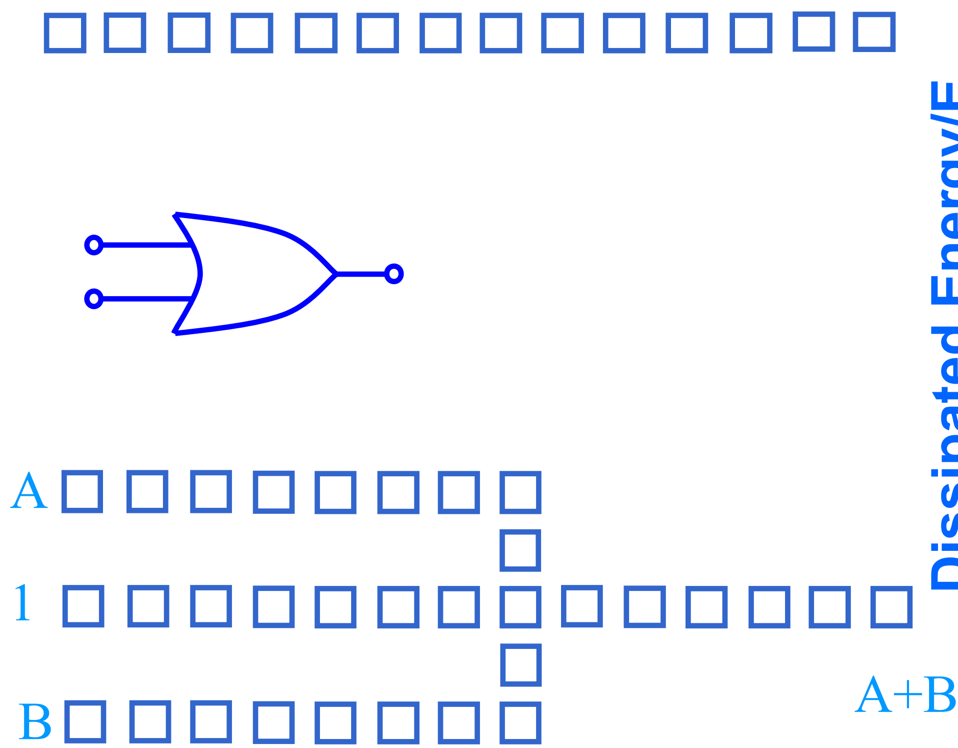
Power Gain in QCA Cells

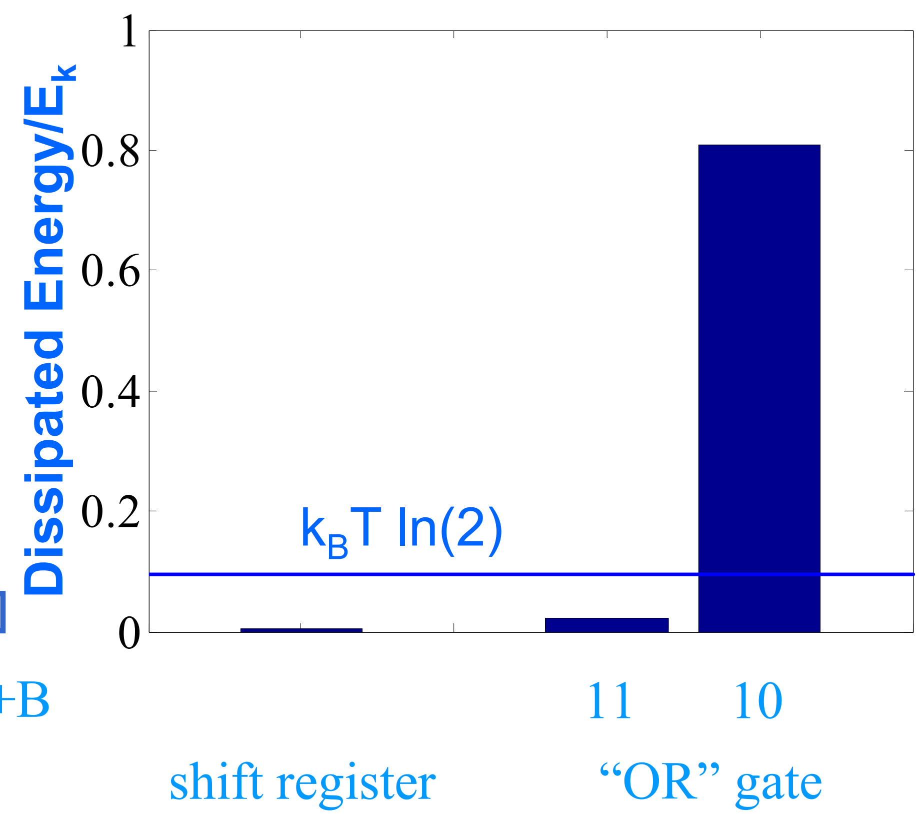
- Power gain is crucial for practical devices because some energy is always lost between stages.
- Lost energy must be replaced.
  - Conventional devices – current from power supply
  - QCA devices – from the clock
- Unity power gain means replacing exactly as much energy as is lost to environment.

Power gain > 3 has been measured in metal-dot QCA.

Landauer Clocking

Energy dissipation in Landauer-clocked circuit





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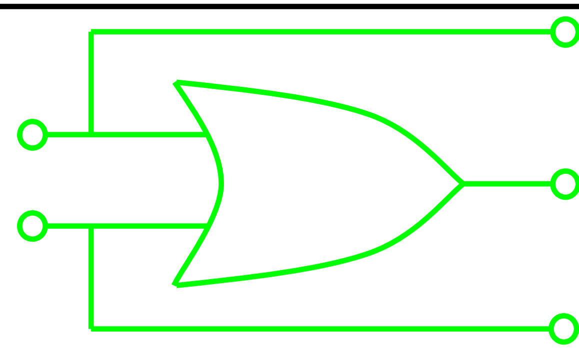
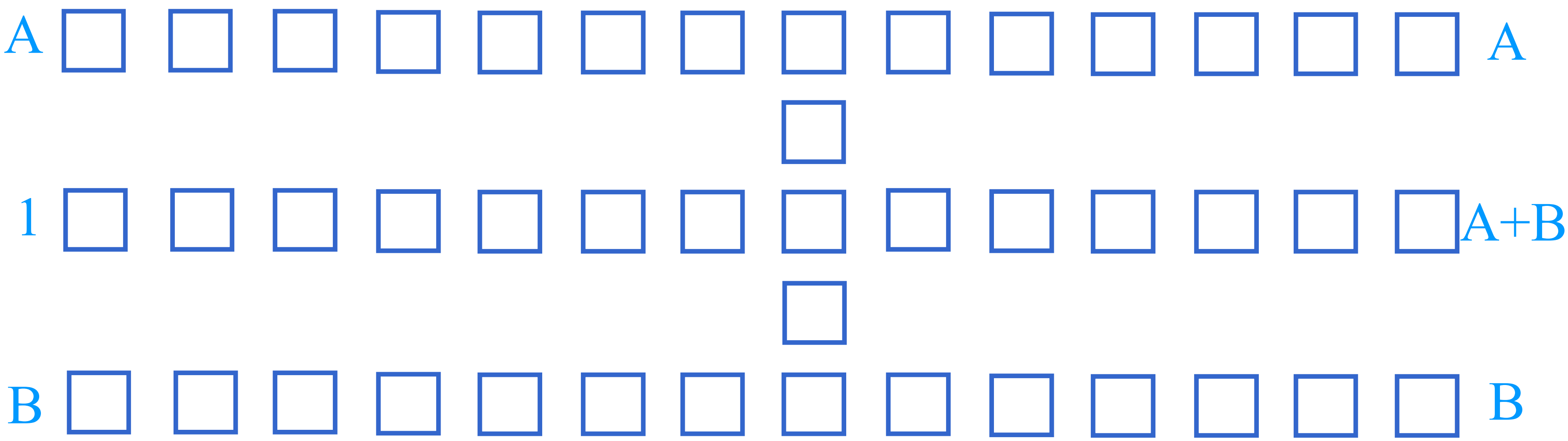
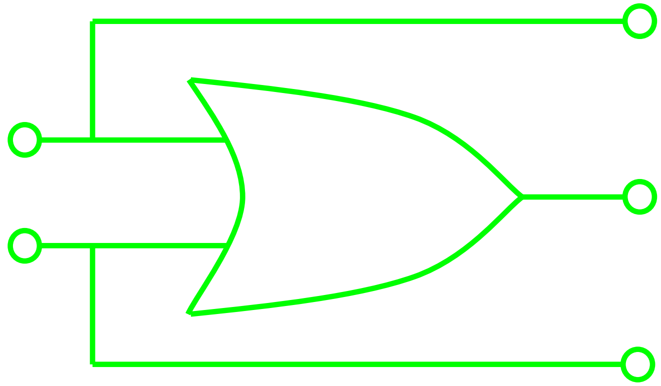
Test circuit: OR gate

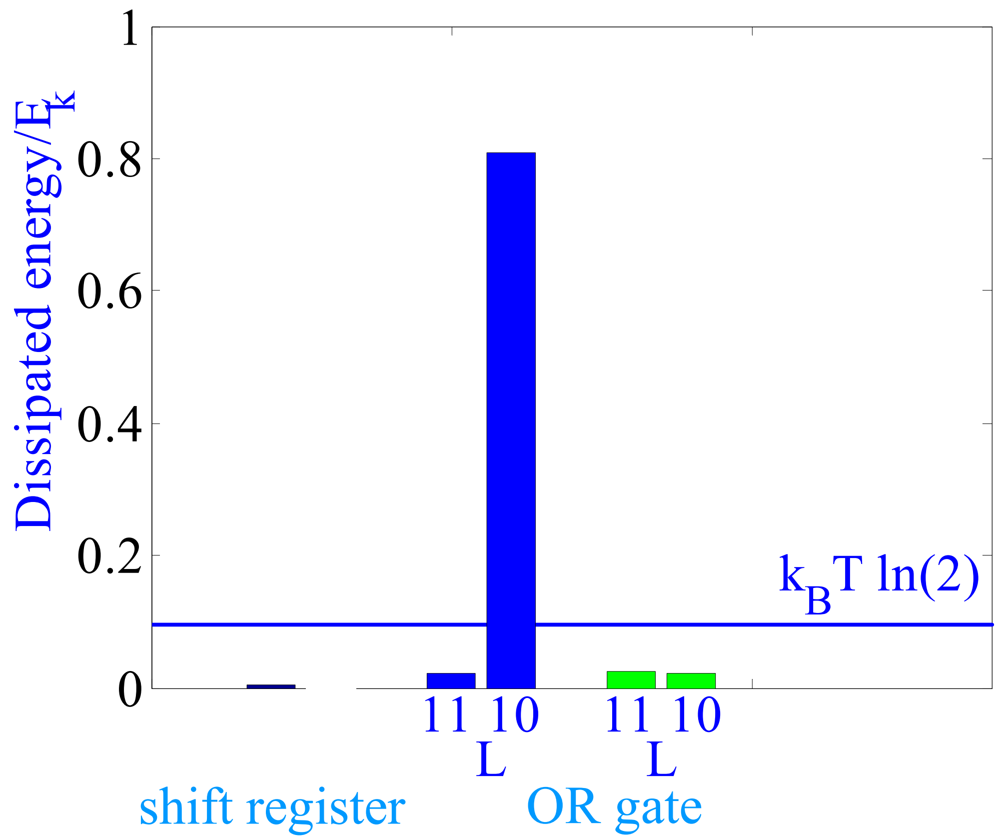




Landauer clocking with echo of inputs to outputs

Energy dissipation in the OR gate





Energy dissipation greatly reduced with inputs echoed to outputs

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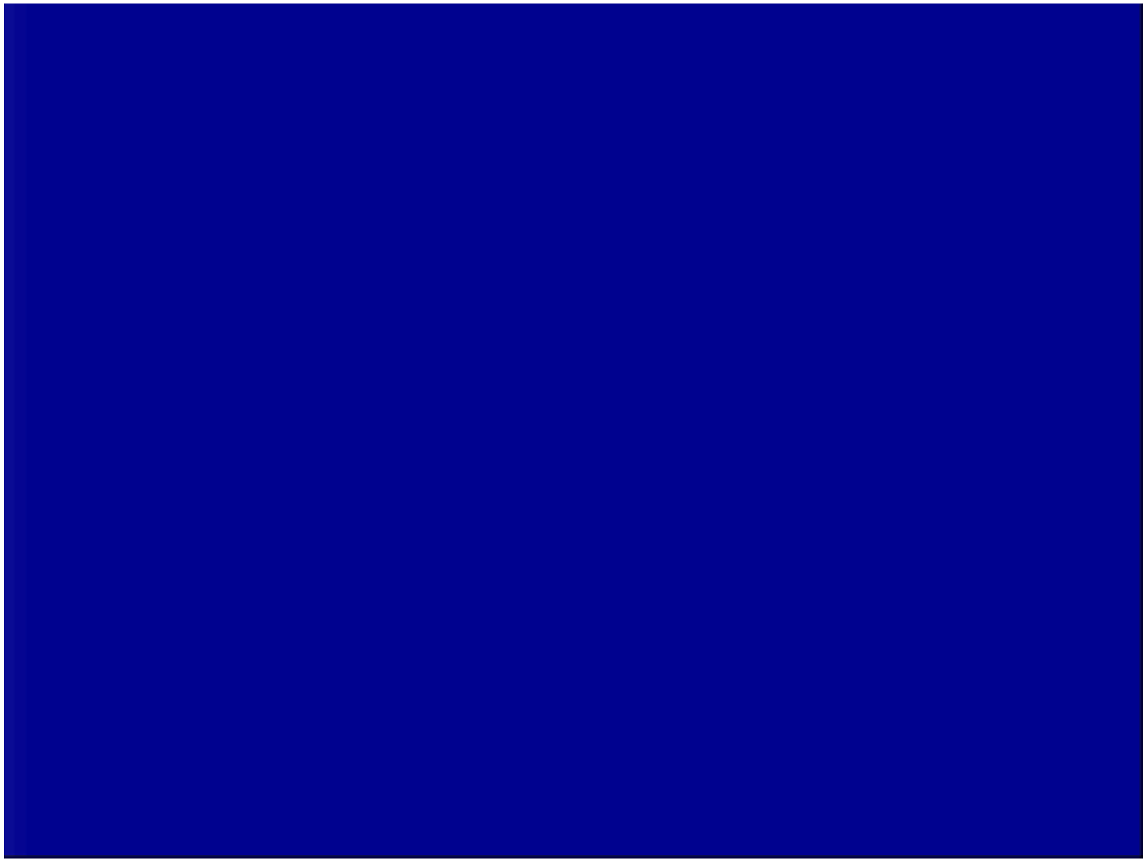
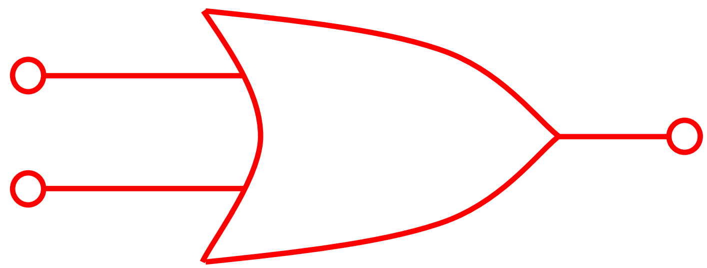
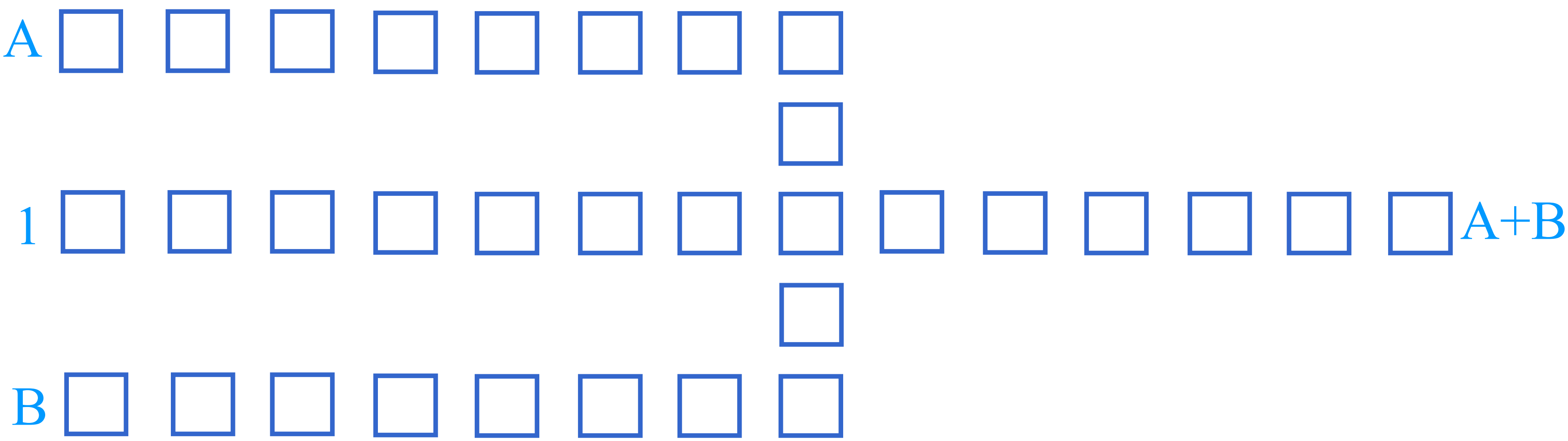
Bennett clocking of QCA



Output is used to erase intermediate results.

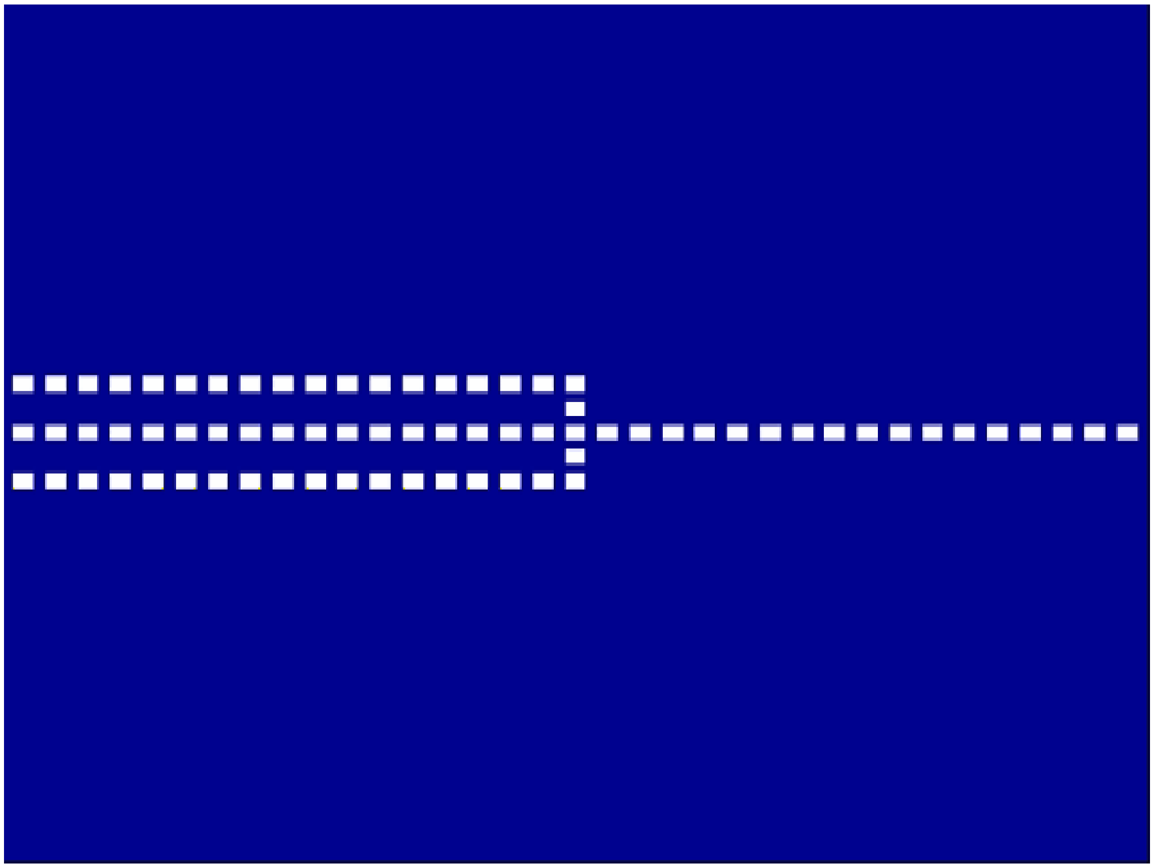
Test circuit: OR gate





Bennett clocked OR gate

Bennett clocking of QCA



For QCA no change in layout is required.

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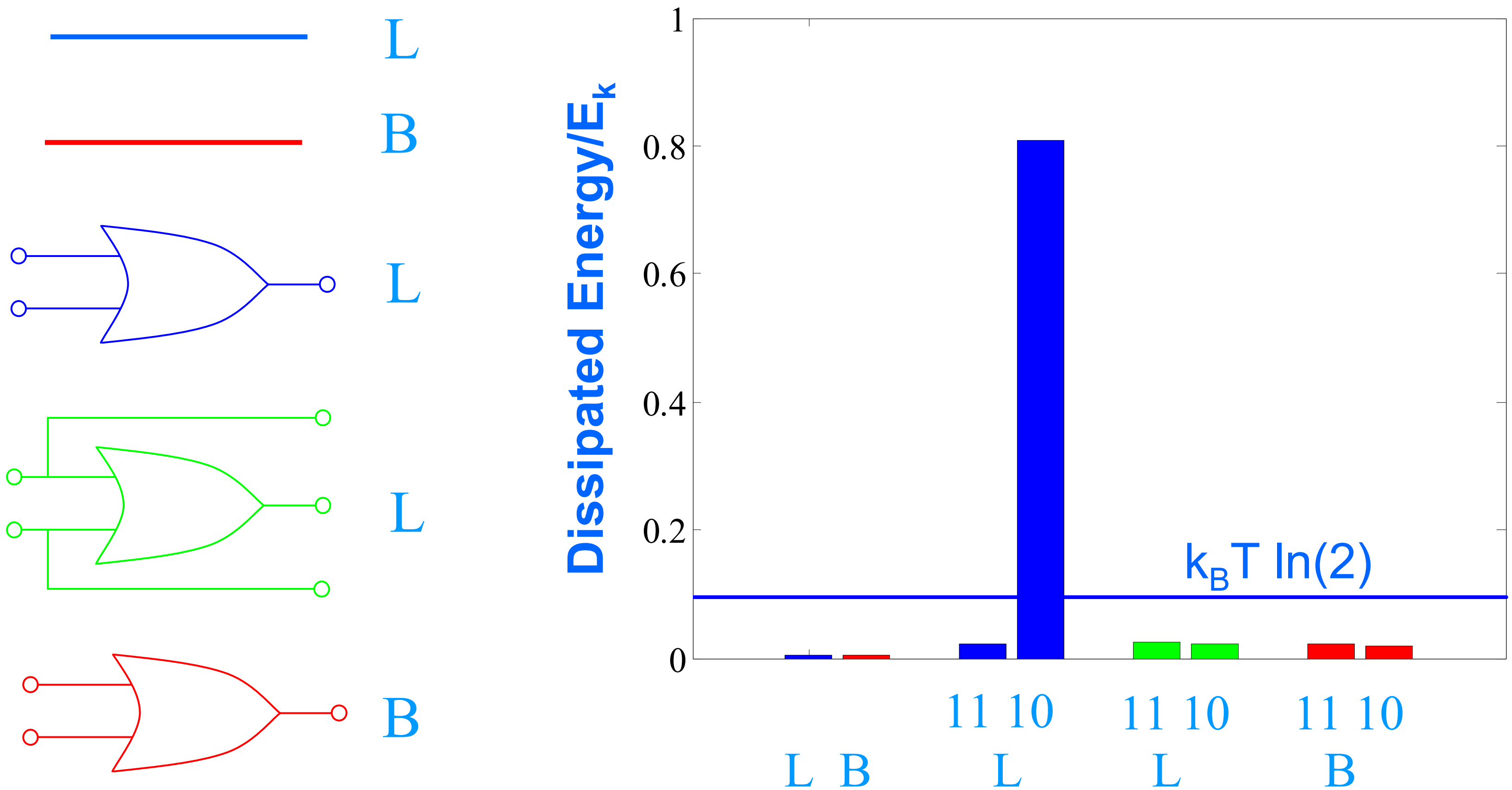
Bennett-style computation may be practical in QCA



Direct time-dependent calculations shows: Logically reversible circuit can dissipate much less than $k_B T \ln(2)$

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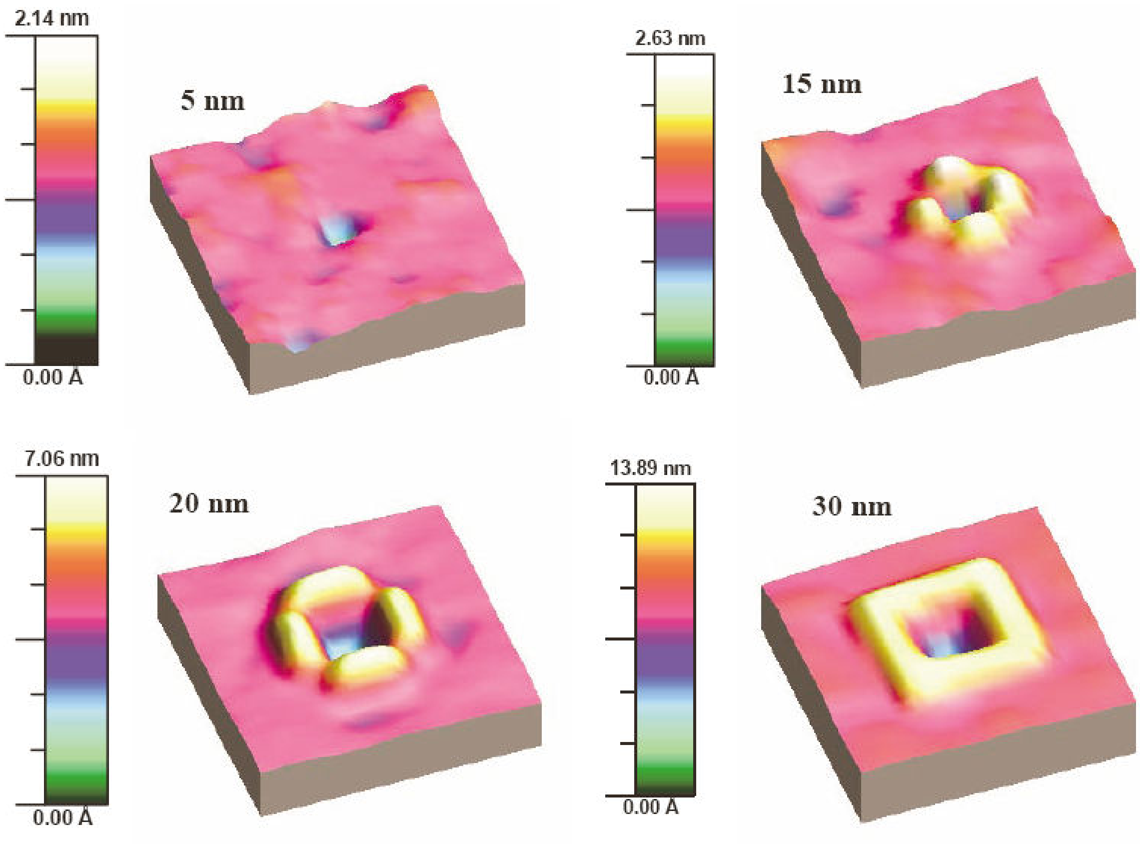
QCA implementations

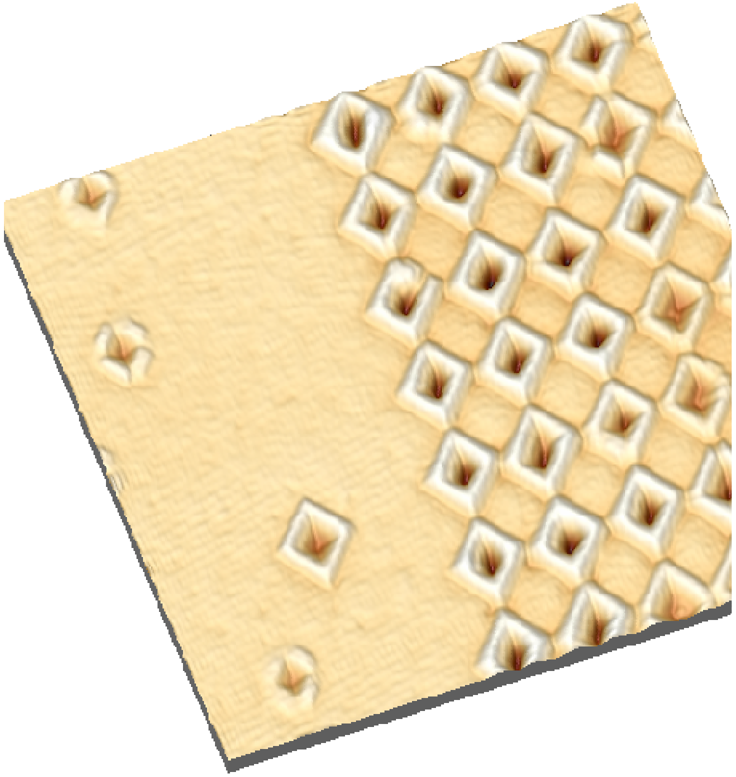
- Semiconductor-dot QCA
  - SiGe quantum fortresses
  - Silicon P-doping
  - GaAs
  - Silicon dot SET’s
- Magnetic QCA
- Metal-dot QCA
- Molecular QCA
- CMOS analogue

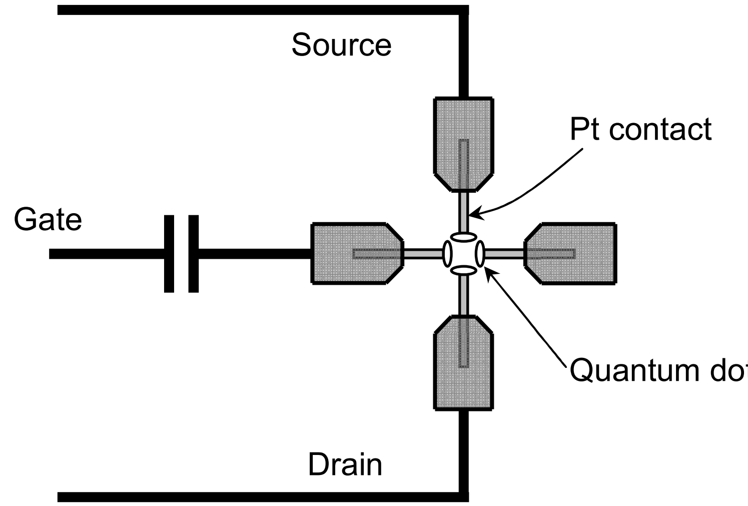
Quantum Fortress Growth

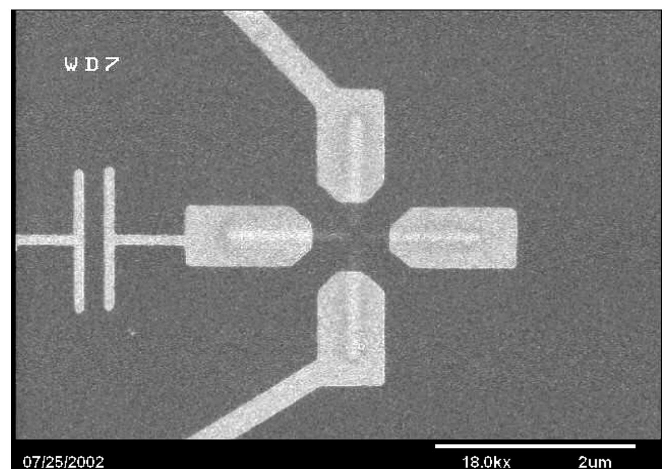


h nm $Ge_{0.3}Si_{0.7}$/Si(100), 550^o C, 0.09 nm/s

Quantum Fortress QCA







FIB are used to deposit Pt contacts to ease the alignment requirements of the E-beam lithography.

Architecture Summary

1. Irreversible
2. Fully Reversible: Landauer Clocking
   - Reversible Components
3. Fully Reversible: Bennett Clocking
   - Possibly Irreversible Components
4. Fully Reversible: Collapsed Bennett
   - General purpose floorplan
   - Size of computation limited only by stack size
5. Partially Reversible: Pipelined Bennett
   - Advantages of reversible combined with higher throughput

Architecture Summary

1. Irreversible

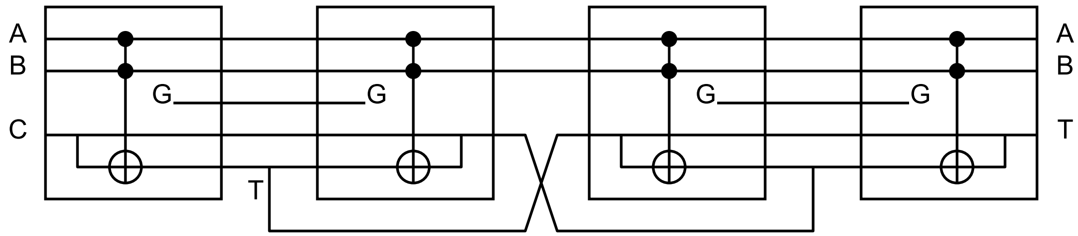
Previous Architecture Work

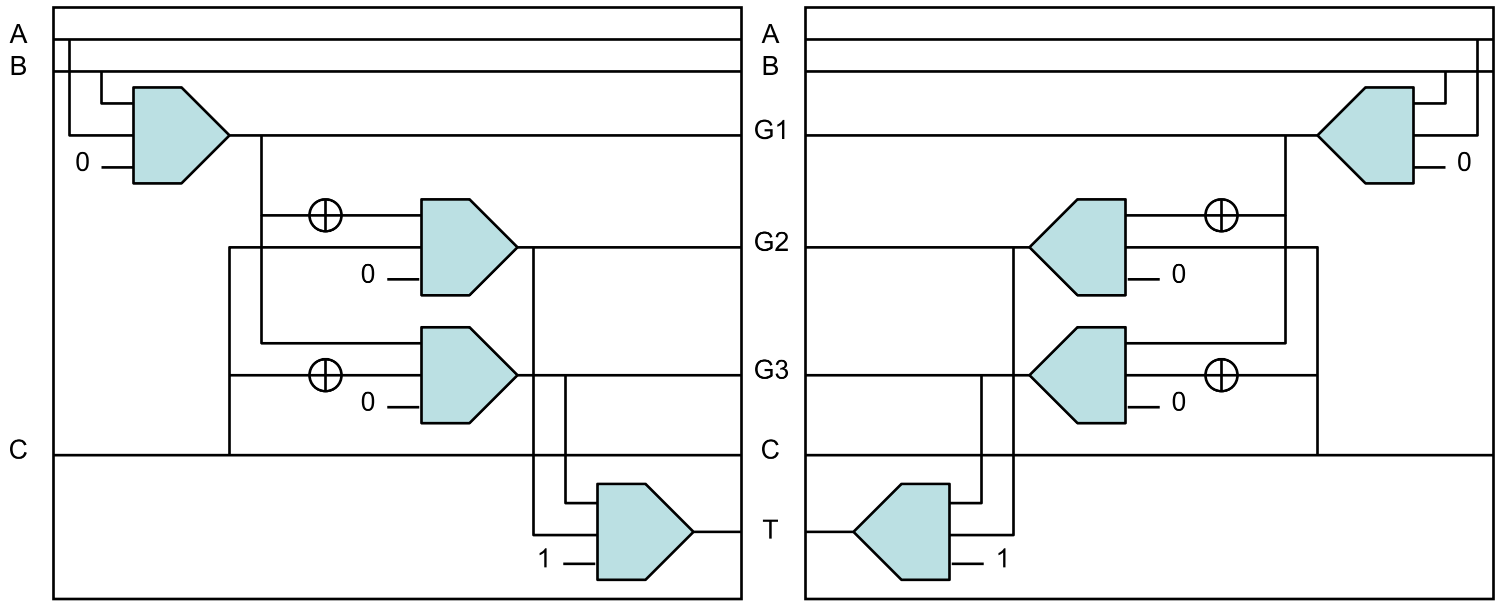
2. Fully Reversible: Landauer Clocking

Lent, et al

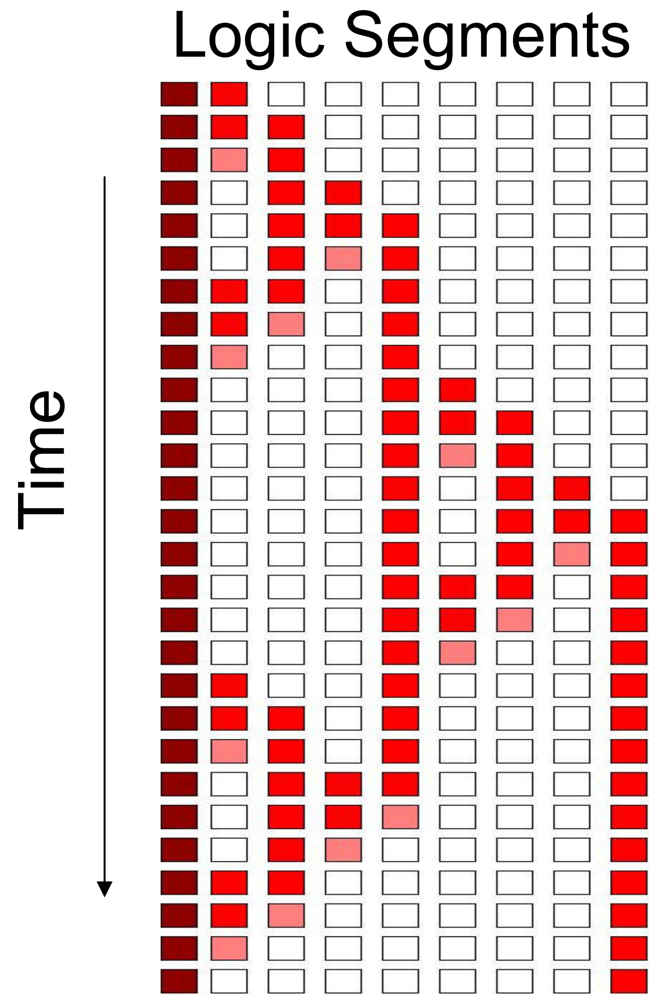
   - Reversible Components
3. Fully Reversible: Bennett Clocking
   - Possibly Irreversible Components
4. Fully Reversible: Collapsed Bennett
   - General purpose floorplan
   - Size of computation limited only by stack size
5. Partially Reversible: Pipelined Bennett
   - Advantages of reversible combined with higher throughput

QDCA Reversible Toffoli



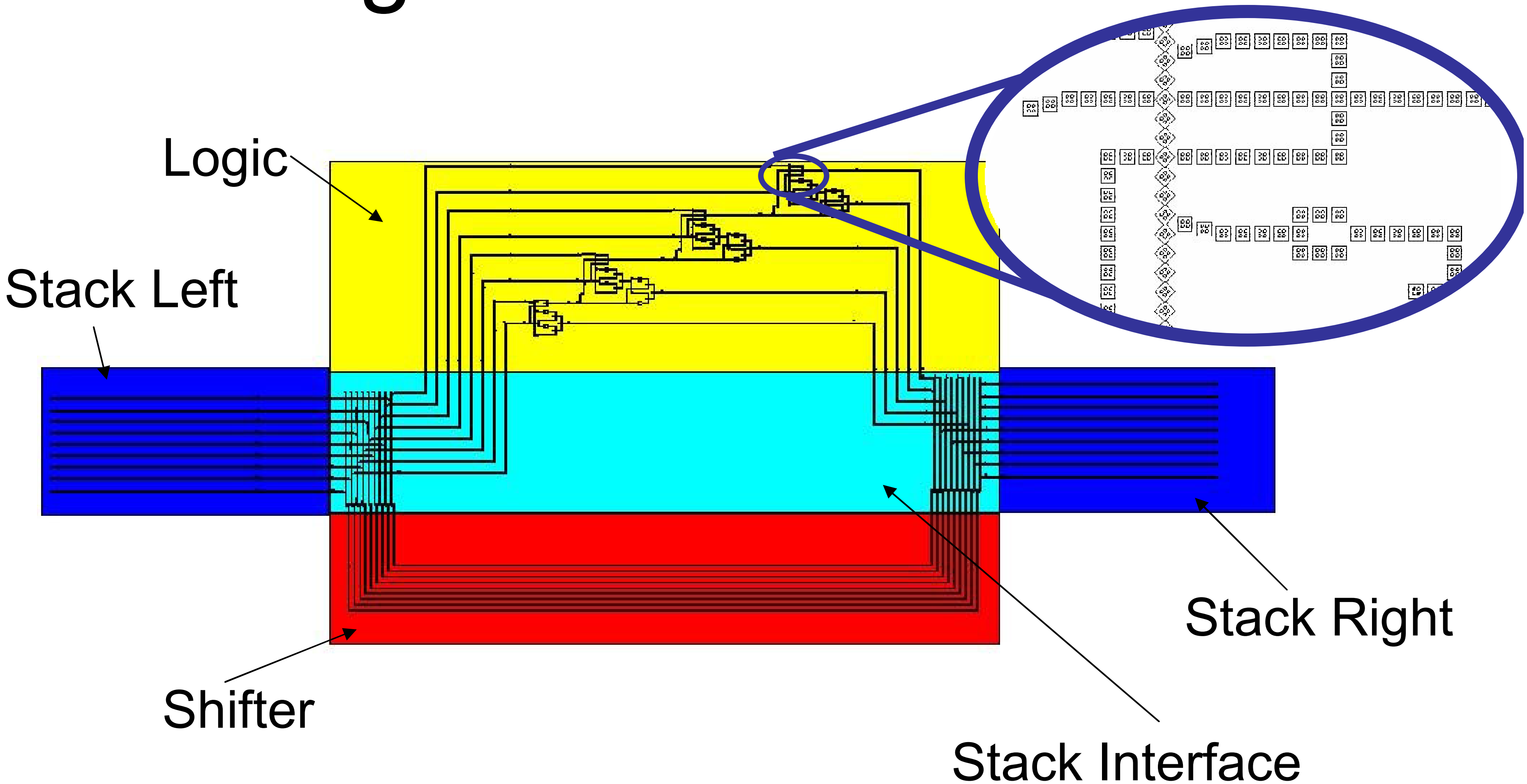


Bennett's Algorithm (1982)



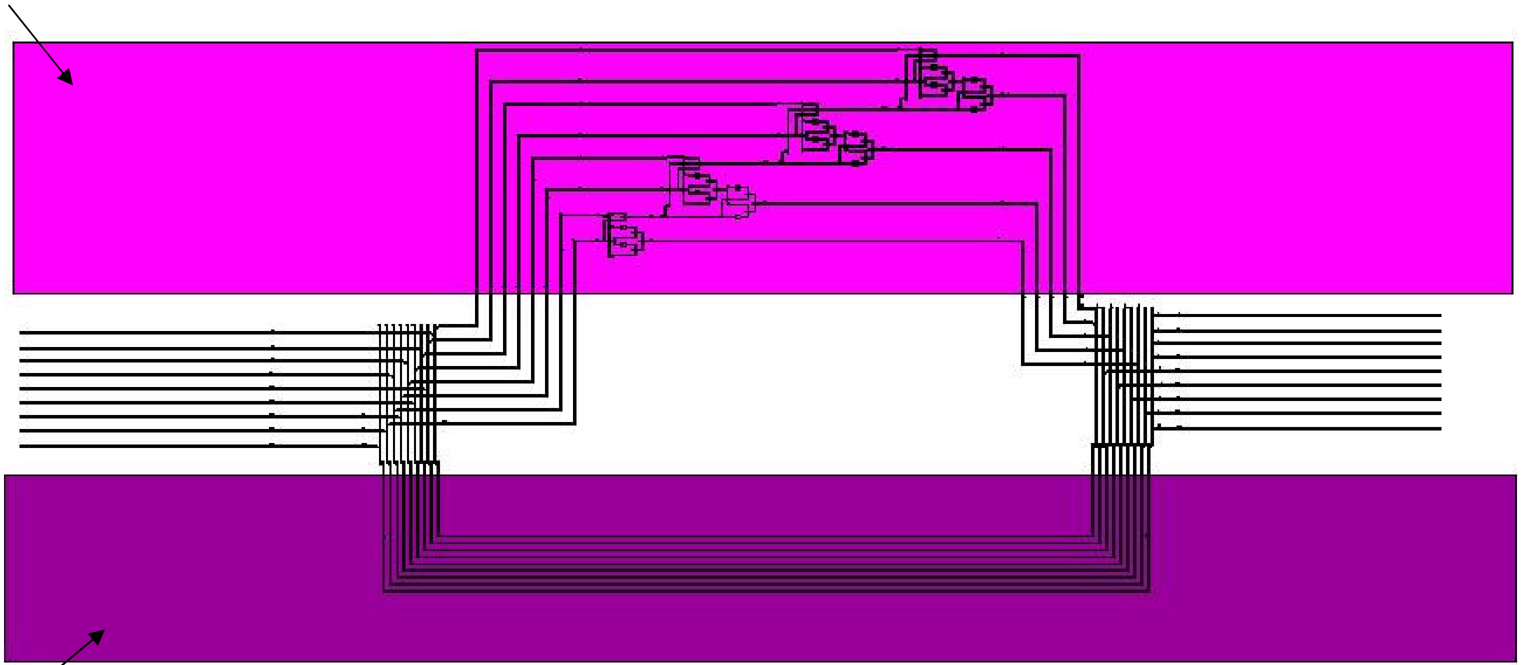
- Original input saved throughout computation
- Intermediate state decomputed when possible
- Intermediate stage can be decomputed only if previous stage is computed
- Final state consists of original input and final output
- For 8 segments, at most 4 checkpoints need to be stored at any given time

Collapsed Bennett Layout: Regions of QCA Circuit



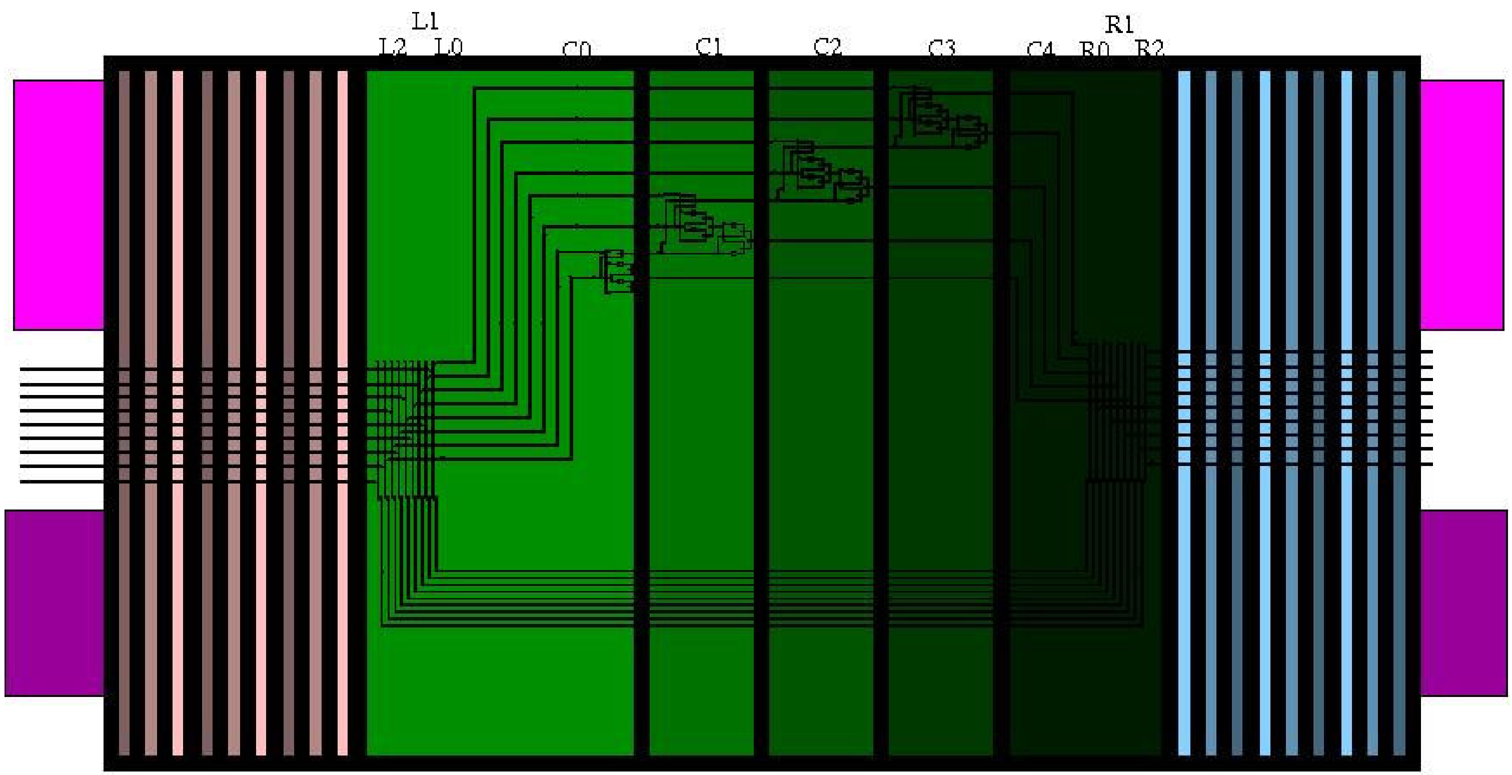
Collapsed Bennett Layout: Disable Regions

Logic Disable

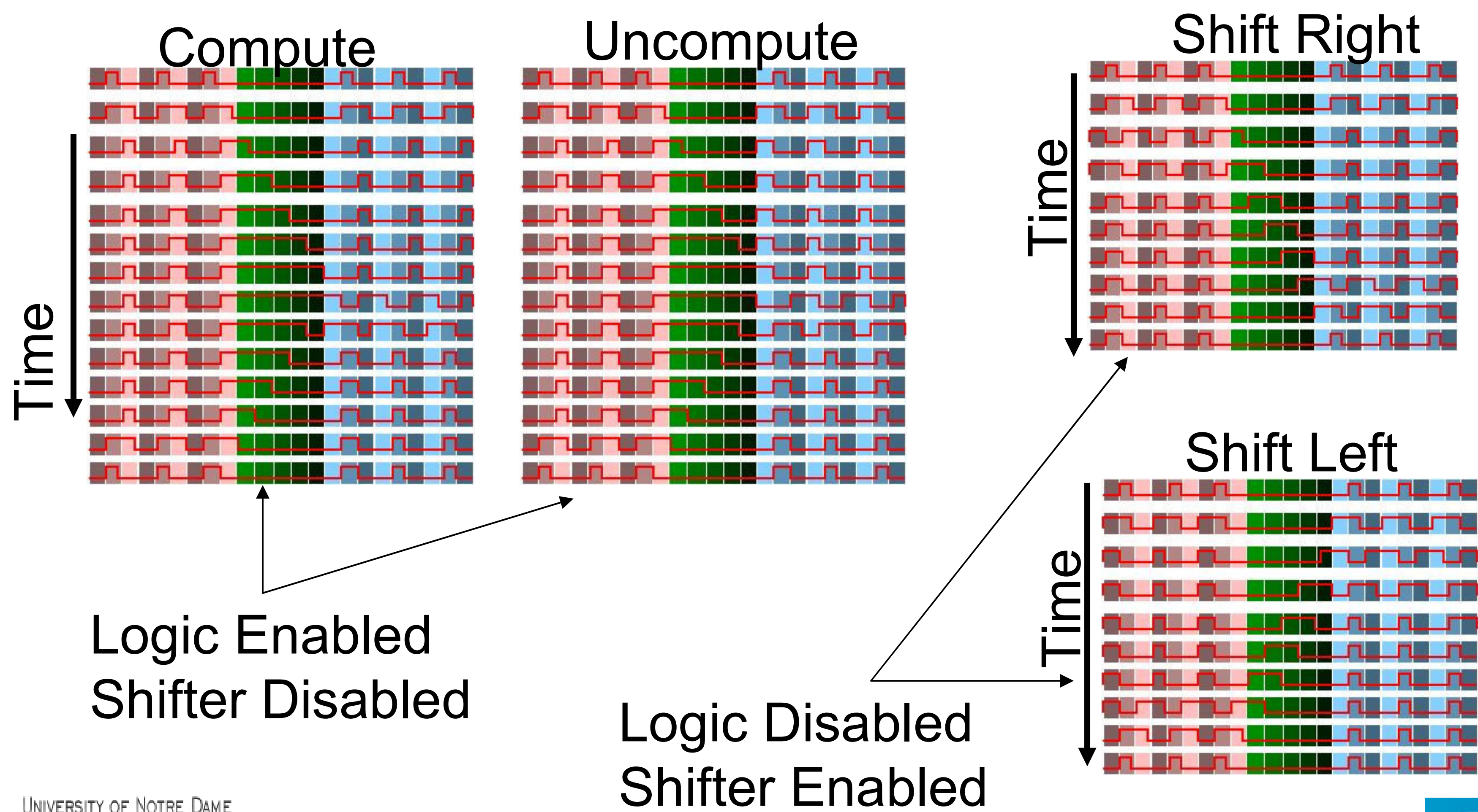


Shift Disable

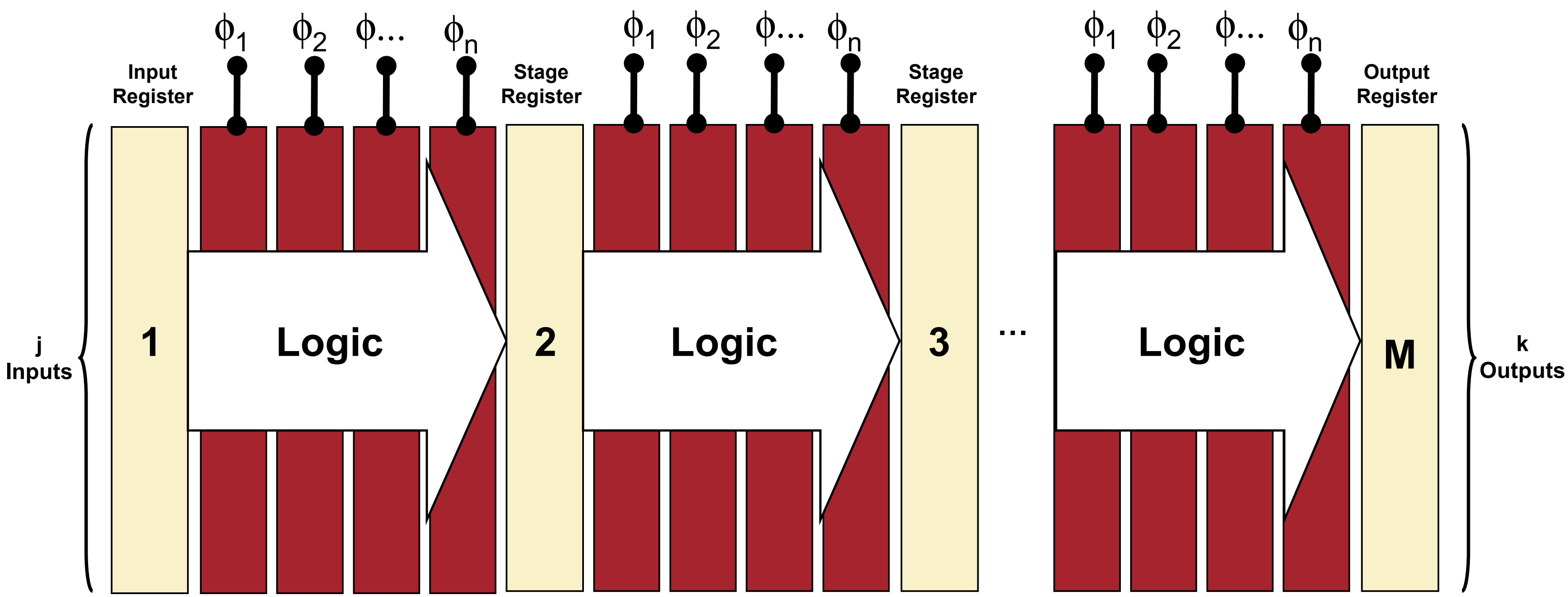
Collapsed Bennett Layout



Collapsed Bennett Layout



Bennett Pipelined: Architecture (Top view)



n clock phases:

ϕ_n = phased signals for Bennett clocking

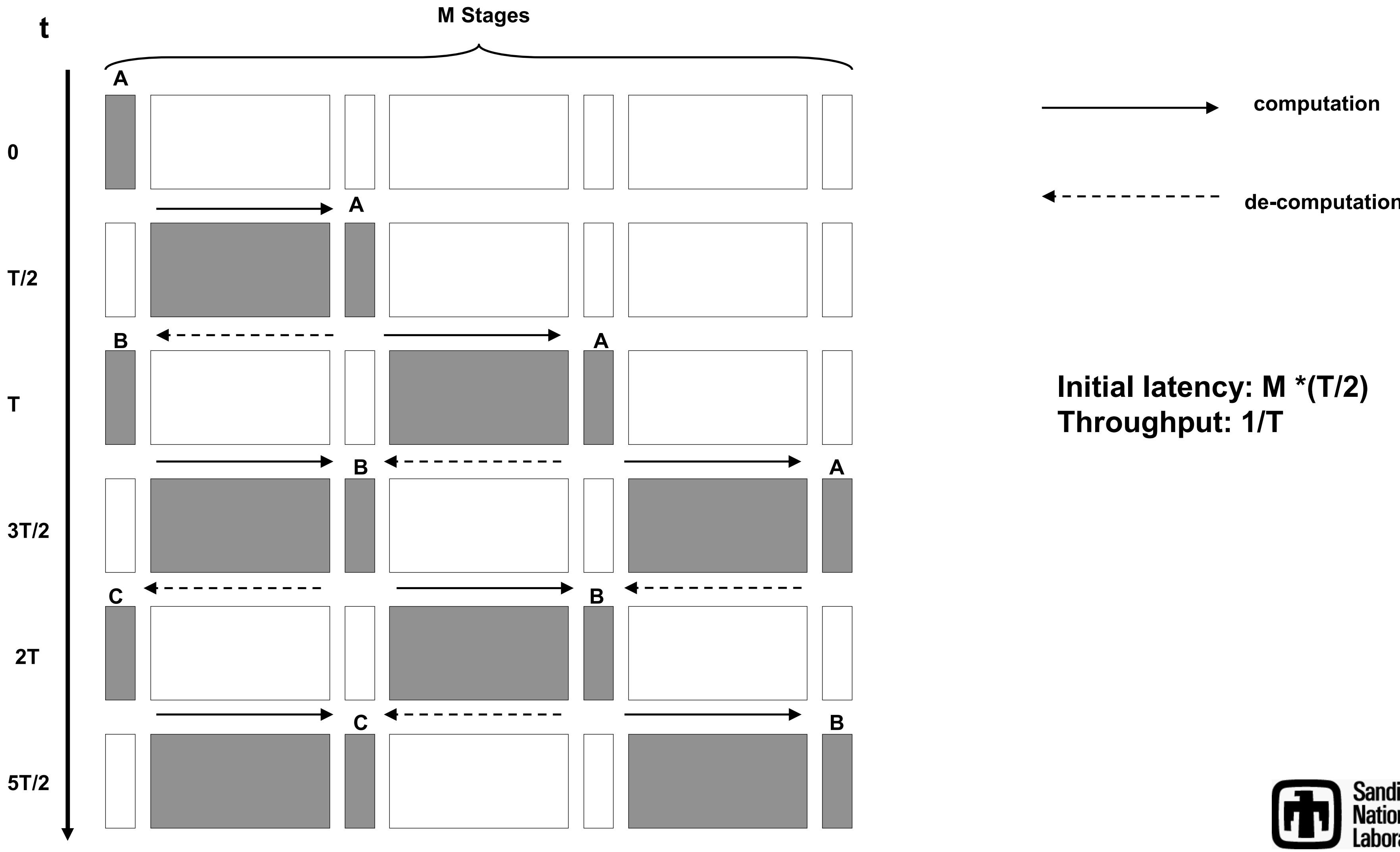
V_{min} :cell released

V_{max} :cell locked

M stages:

Bennett zones + Registers

Data pipelining



Initial latency: M *(T/2)
Throughput: 1/T

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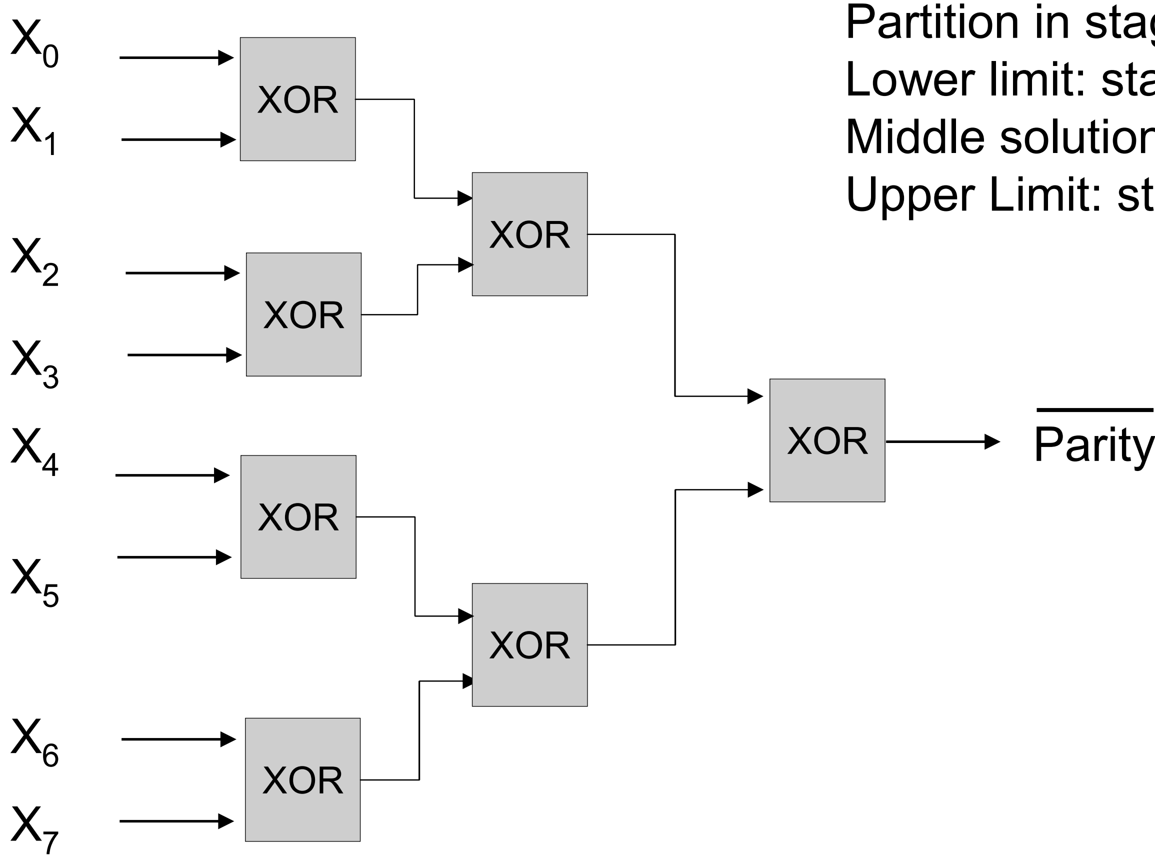
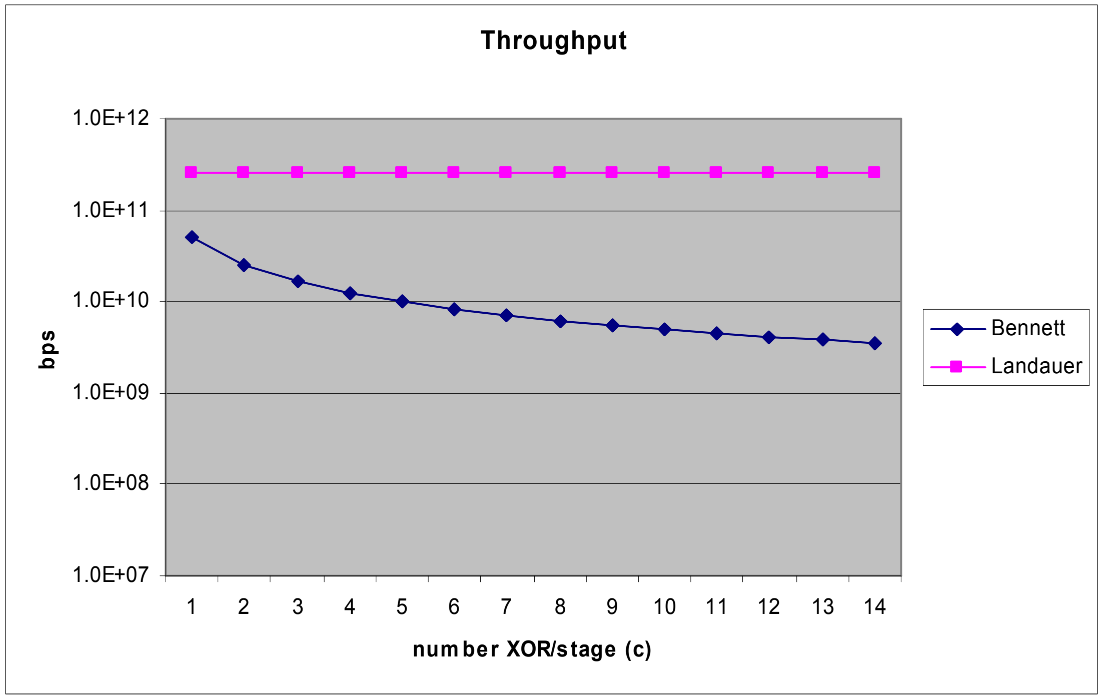
Case study: XOR Tree

M stages parity checker



Partition in stages:
Lower limit: stage size = 2 QCA cell
Middle solution: stage size = 1 XOR GATE
Upper Limit: stage size = M XOR gates

Performance evaluations



- Landauer scheme shows higher throughput and the gap between the performances increases with the increase of c (c=14 only one Bennett stage). (note: c=1not same as Landauer due to the size of the basic stage)

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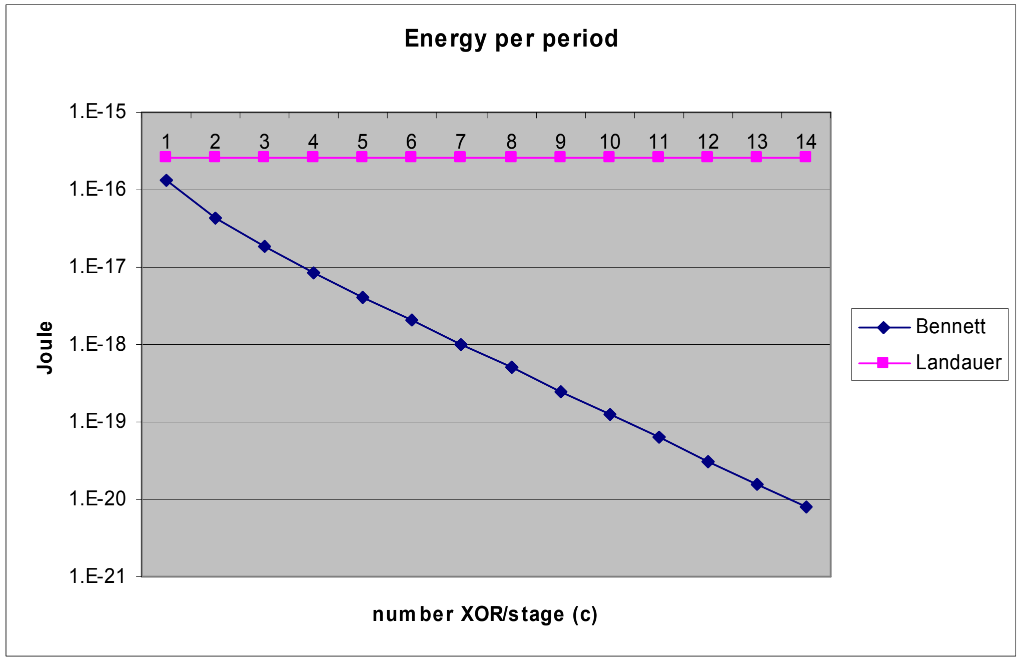
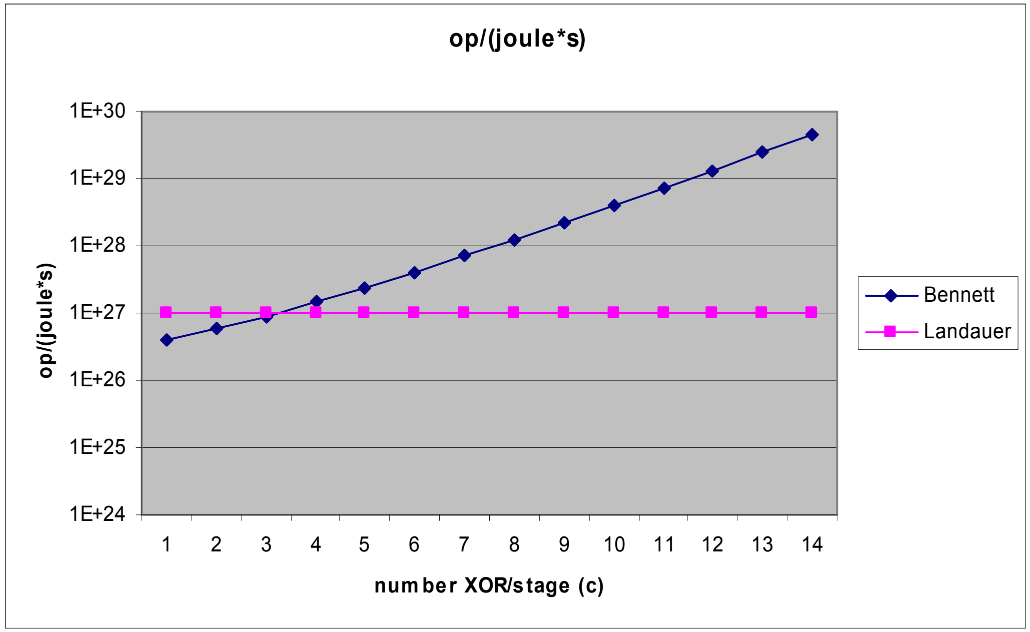
Performance evaluations



- The improvement in terms of power consumption becomes better with the increase of c (note: the power dissipated also with a pure Bennett scheme c=14 does not become zero as the inputs to the whole circuit are still deleted every T)

Performance evaluations



- "Given a second of time and a Joule of energy, what is the amount of operations (output bits) obtained?"
- The result shows an intersection of the two curves:
  - c< 3 Landauer clocking has better performances
  - c>3 Bennett clocking behaves better

Silicon P-dot QCA cell

APPLIED PHYSICS LETTERS **89**, 013503 (2006)

Demonstration of a silicon-based quantum cellular automata cell

M. Mitic,[a] M. C. Cassidy, K. D. Petersson,[b] R. P. Starrett, E. Gauja, R. Brenner, R. G. Clark, and A. S. Dzurak
Centre for Quantum Computer Technology, School of Electrical Engineering and School of Physics, The University of New South Wales, Sydney, New South Wales 2052, Australia

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Centre for Quantum Computer Technology, School of Physics, University of Melbourne, Victoria 3010, Australia

(Received 8 March 2006; accepted 18 May 2006; published online 5 July 2006)

We report on the demonstration of a silicon-based quantum cellular automata (QCA) unit cell incorporating two pairs of metallically doped (n^+) phosphorus-implanted nanoscale dots, separated from source and drain reservoirs by nominally undoped tunnel barriers. Metallic cell control gates, together with Al–AlO$_x$ single electron transistors for noninvasive cell-state readout, are located on the device surface and capacitively coupled to the buried QCA cell. Operation at subkelvin temperatures was demonstrated by switching of a single electron between output dots, induced by a driven single electron transfer in the input dots. The stability limits of the QCA cell operation were also determined. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2219128]

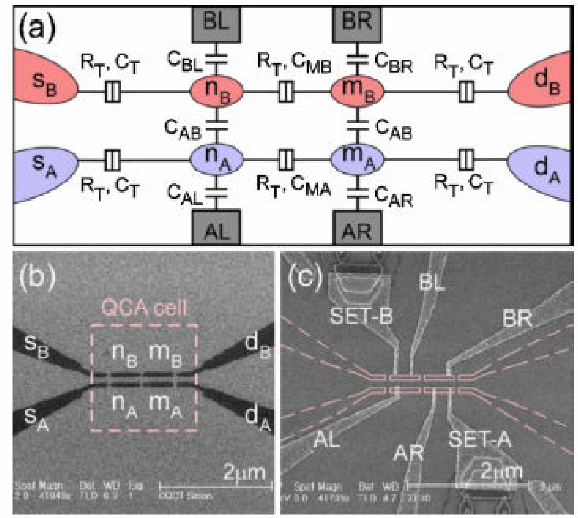
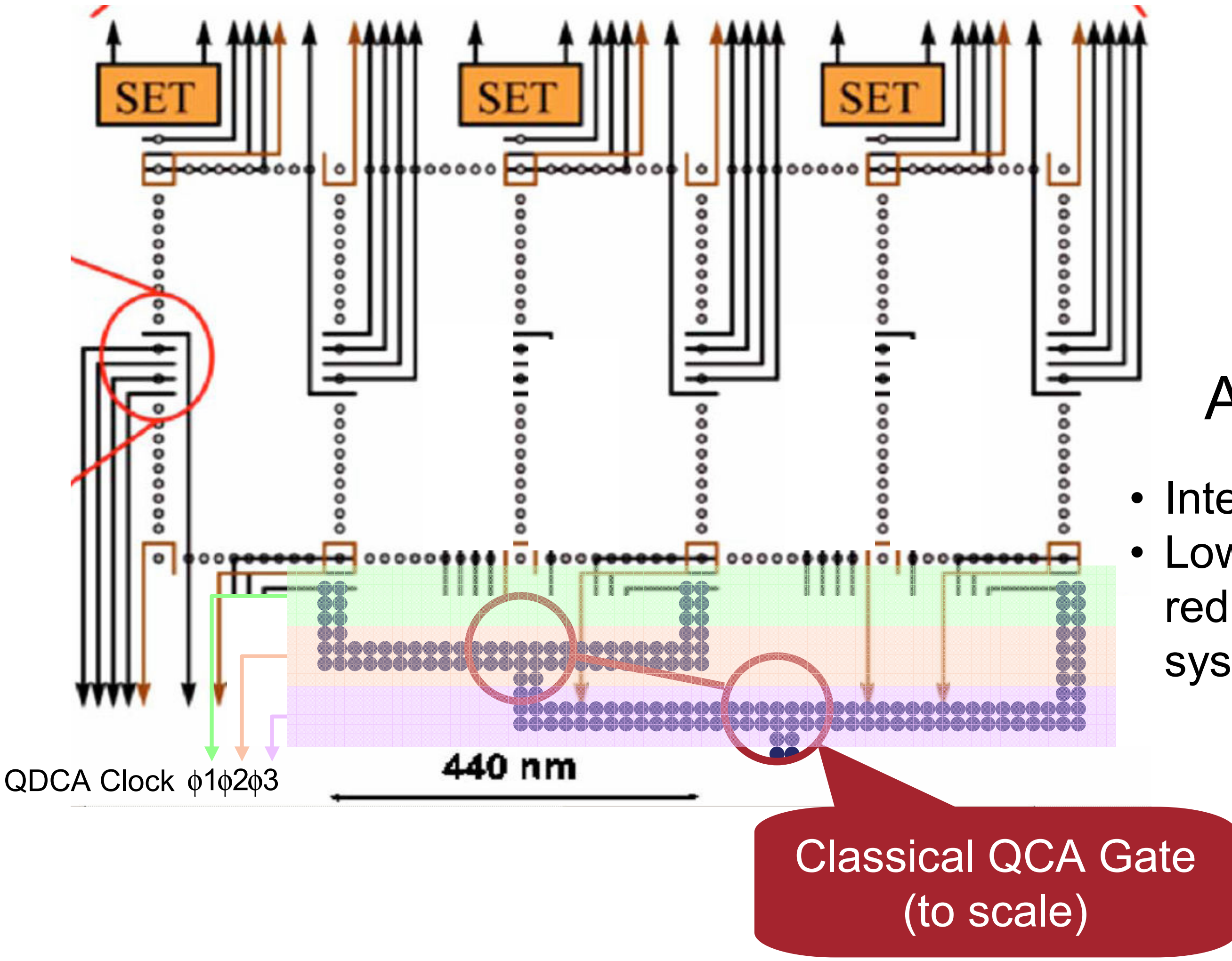


FIG. 1. (Color online) (a) Simplified circuit equivalent of the QCA cell, (b) SEM image of phosphorus-implanted n^+ regions (dark in image), and (c) SEM image of completed device. The buried n^+ dots and leads are marked using dashed lines.

- Dots defined by implanted phosphorus
- Single-donor creation foreseen
- Direct measurement of cell switching

QDCA Logic Directly Attached to QC

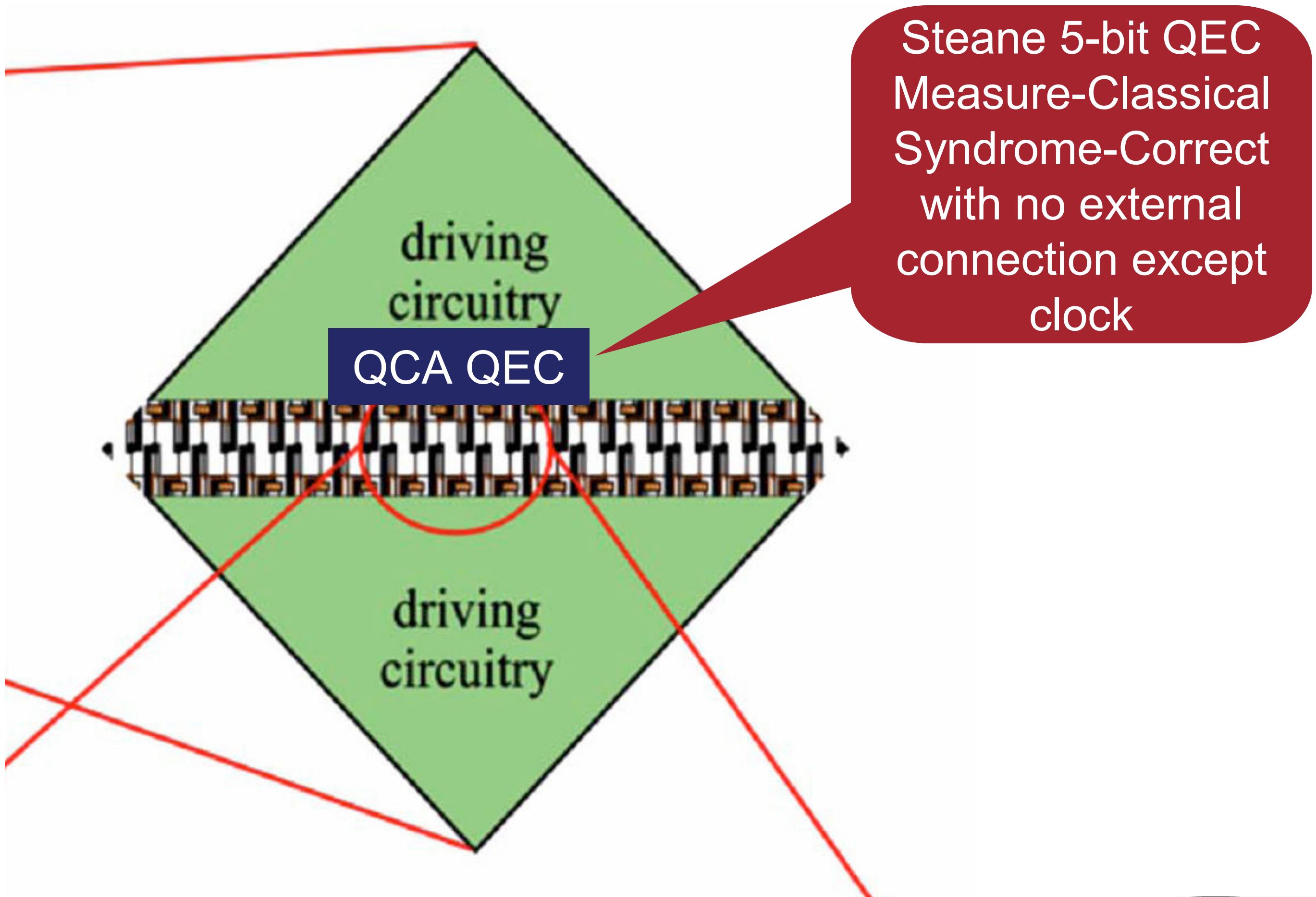


Advantages:

- Integration on one substrate
- Low power dissipation reduces load on cooling system

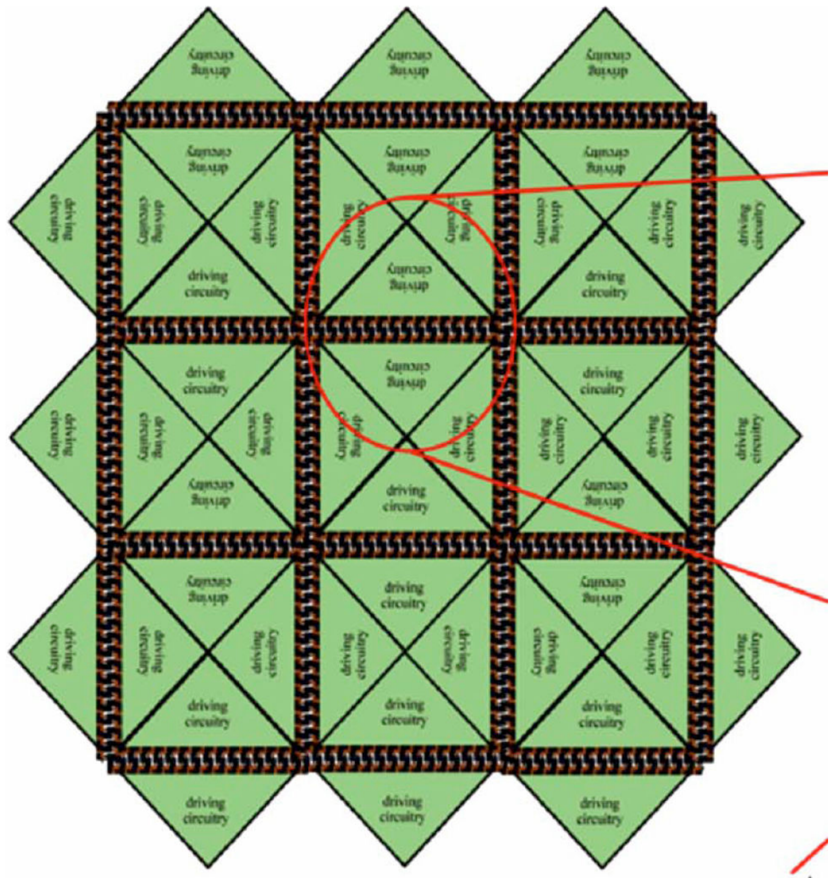
Base diagram from Physical Review B 74, 045311 2006,
Two-dimensional architectures for donor-based quantum computing

Self-Contained Classical+Quantum Logic



Base diagram from Physical Review B 74, 045311 2006,
Two-dimensional architectures for donor-based quantum computing

Large QC and QCA Arrays

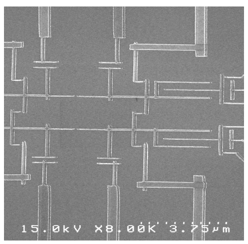


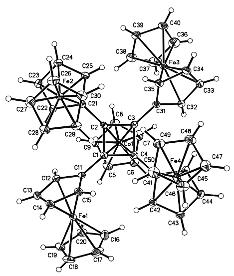
Advantages

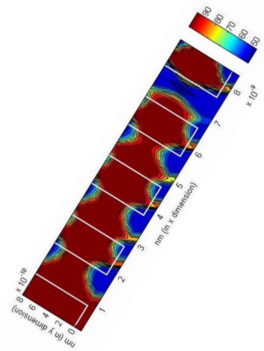
- QCA logic “lives” in the single electron world, thus avoiding the need to amplify single electron signals to CMOS levels
- QCA logic would be used to execute the classical part of QEC recovery mechanisms, which is most (e. g. 99%) of the activity in a projected QC
- Each QCA “island” would consume less resources than SET, amplifier, bonding pad, and cable to controller through cryostat it replaces
- QCA would allow the classical circuitry to be implemented on-chip without over-heating the dilution refrigerator.

System + Application Architectures

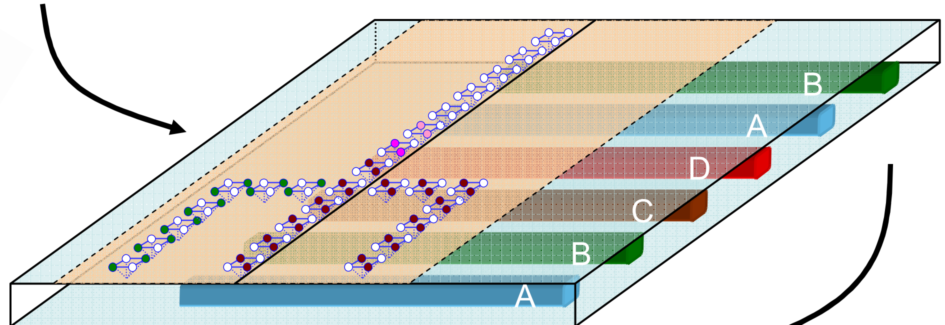
Grounded in device physics & simulation





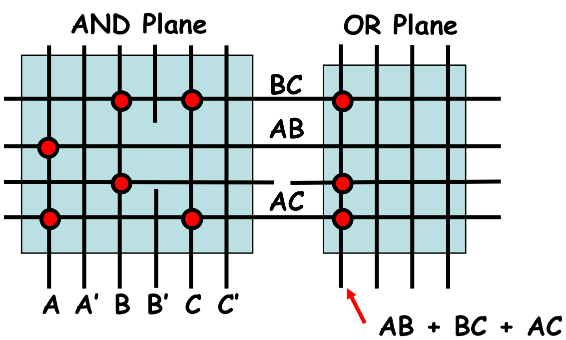


Incorporate clock driven dataflow

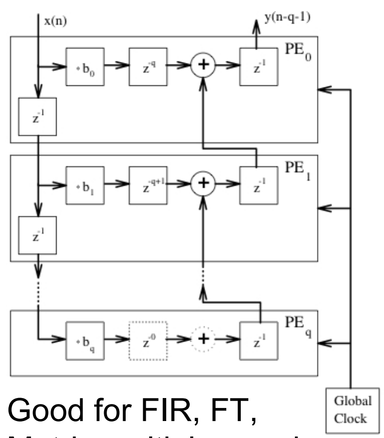


Device architecture maps well to many system architectures…

Reconfigurable

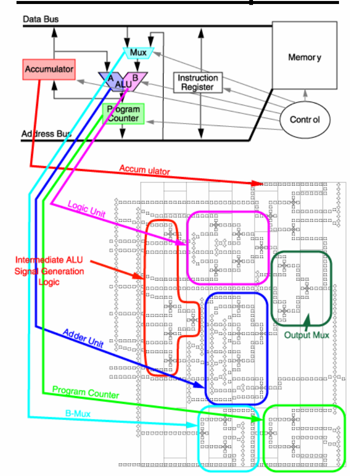


Systolic



Good for FIR, FT, Matrix multiply, graph algorithms, etc.

General Purpose



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Simulations

New devices **New circuits** **New architectures**	⇔	**New simulators**

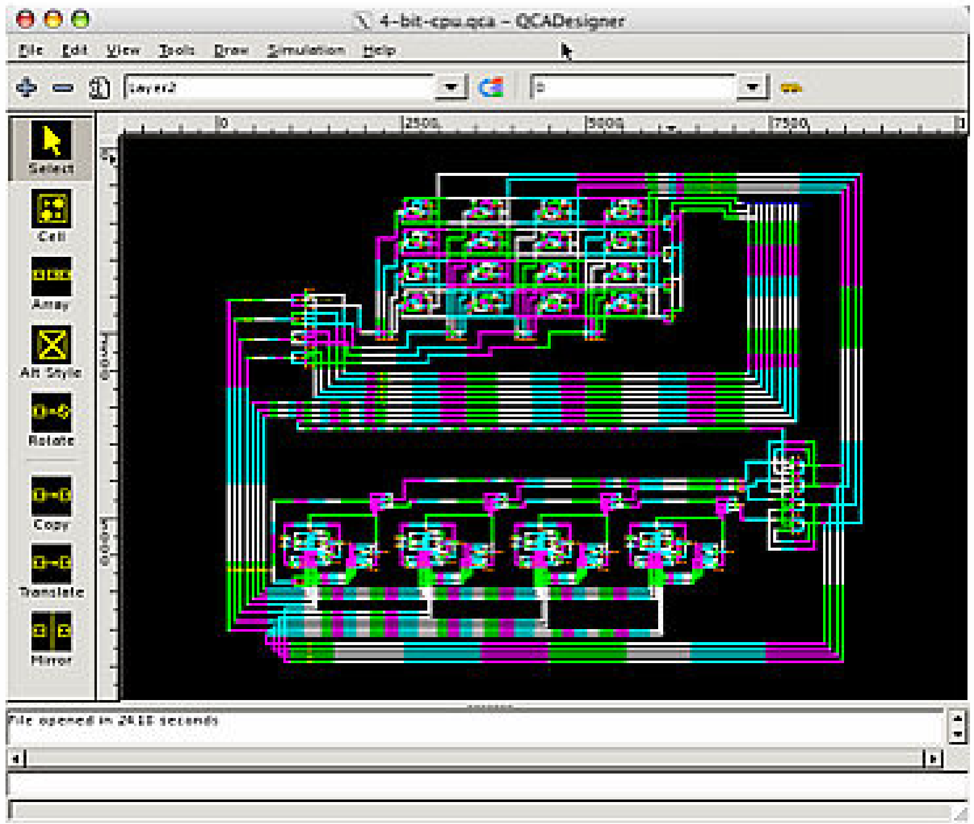
Simulation levels

1) Quantum chemistry
   Ab initio, all-electron, and approx.
2) Density matrix (coherence vector)
   Quantum, dynamic, thermal effects, dissipation
3) Time-independent Schrod. Eq.
4) Semiclassical thermodynamic
5) Logic level
6) Architecture level

slow

fast

QCA design tools



QCADesigner screenshot showing a simple 4-bit processor layout.

QCADesigner

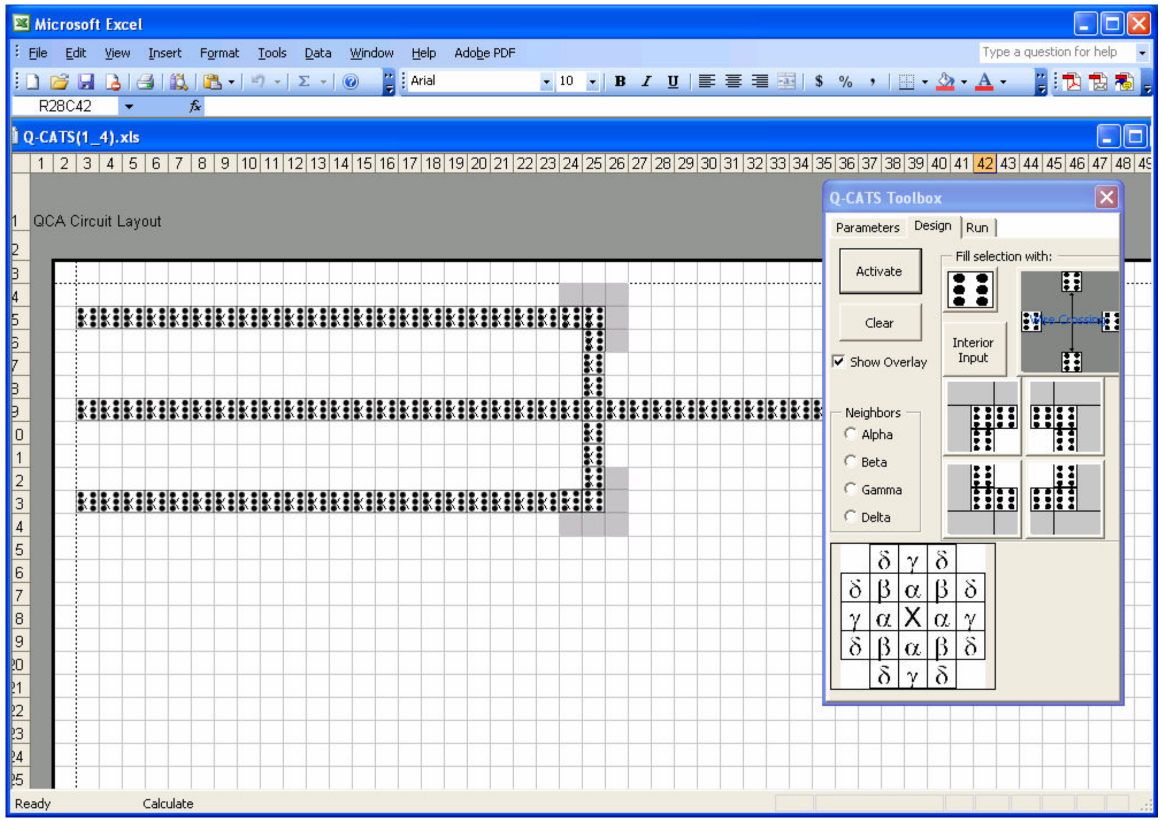
Konrad Walus
U. British Columbia

QCA design tools

QCATS

<u>Q</u>CA
<u>T</u>hermodynamic
<u>S</u>imulator

Semiclassical



Under development

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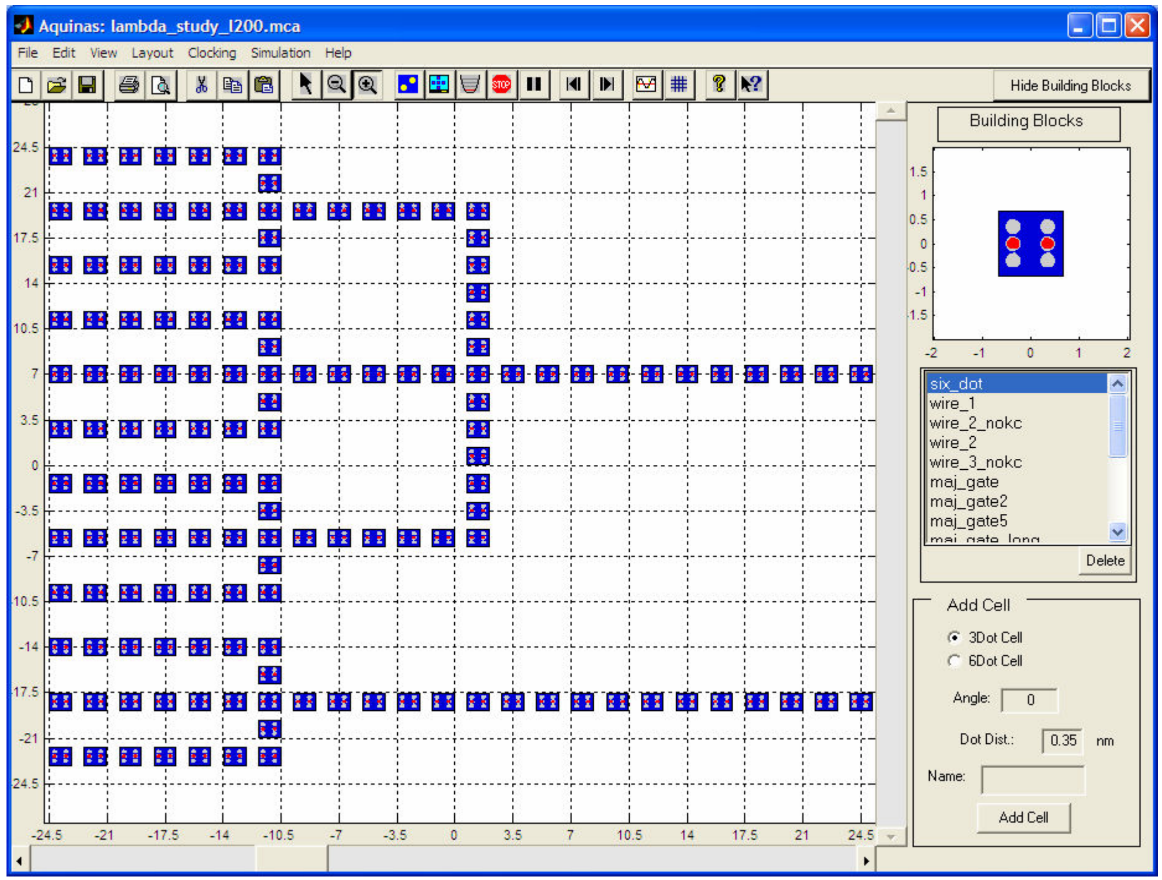
M-AQUINAS

Molecular version of A QUantum Interconnected Network Array Simulator

- GUI allows point-and-click and drag-and-drop editing of QCA circuits.
- Schrödinger solver coupled to local clocking field.



Authors: Enrique Blair
Amy DeCelles

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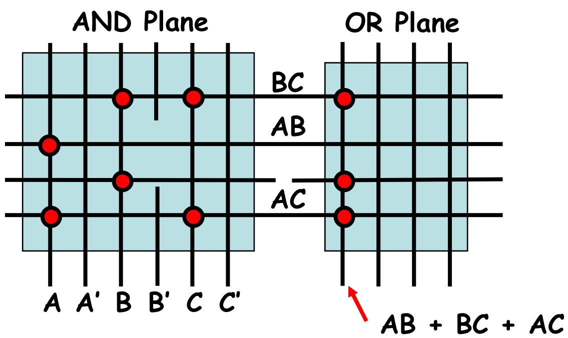
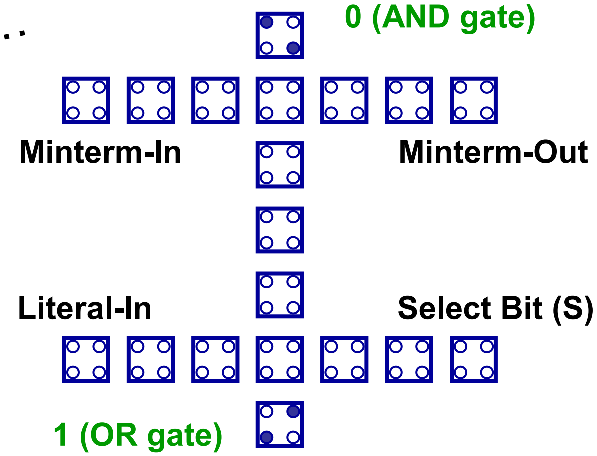
Simulation hierarchies

Architectural-level



+ Logic-level…

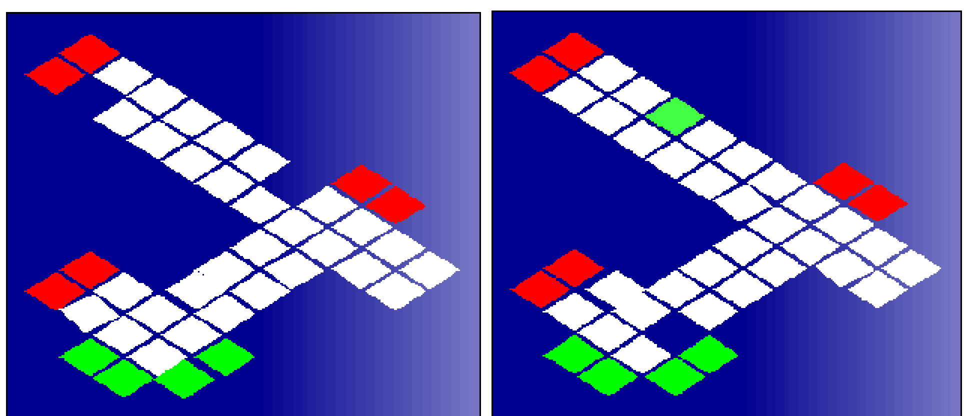


+ device-level…

Minterm-In

Literal-In

Select Bit (S)



pla-defective3.avi

pla-defective2.avi

= Application-level performance metrics

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Conclusions

- Power is a problem for logic today, and it is related to an approach to thermodynamic limits on computing
- However, these limits are due in part to historical choices that can be circumvented
  - Requires new basis for logic
  - Requires new devices, notably devices that handle information and heat differently

- Also: A tie in to coherent quantum computing

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Partnership Opportunity

- This is a project under NINE and SBET
  - We are advocating research in
    - Computing beyond the limits of CMOS
    - Physics of information processing
  - The overall project's deliverables to Sandia are to bootstrap multiple projects in
    - Physical science
    - Information science
    - Simulation
  - We've tried to outline opportunity and expose Sandia to willing partners

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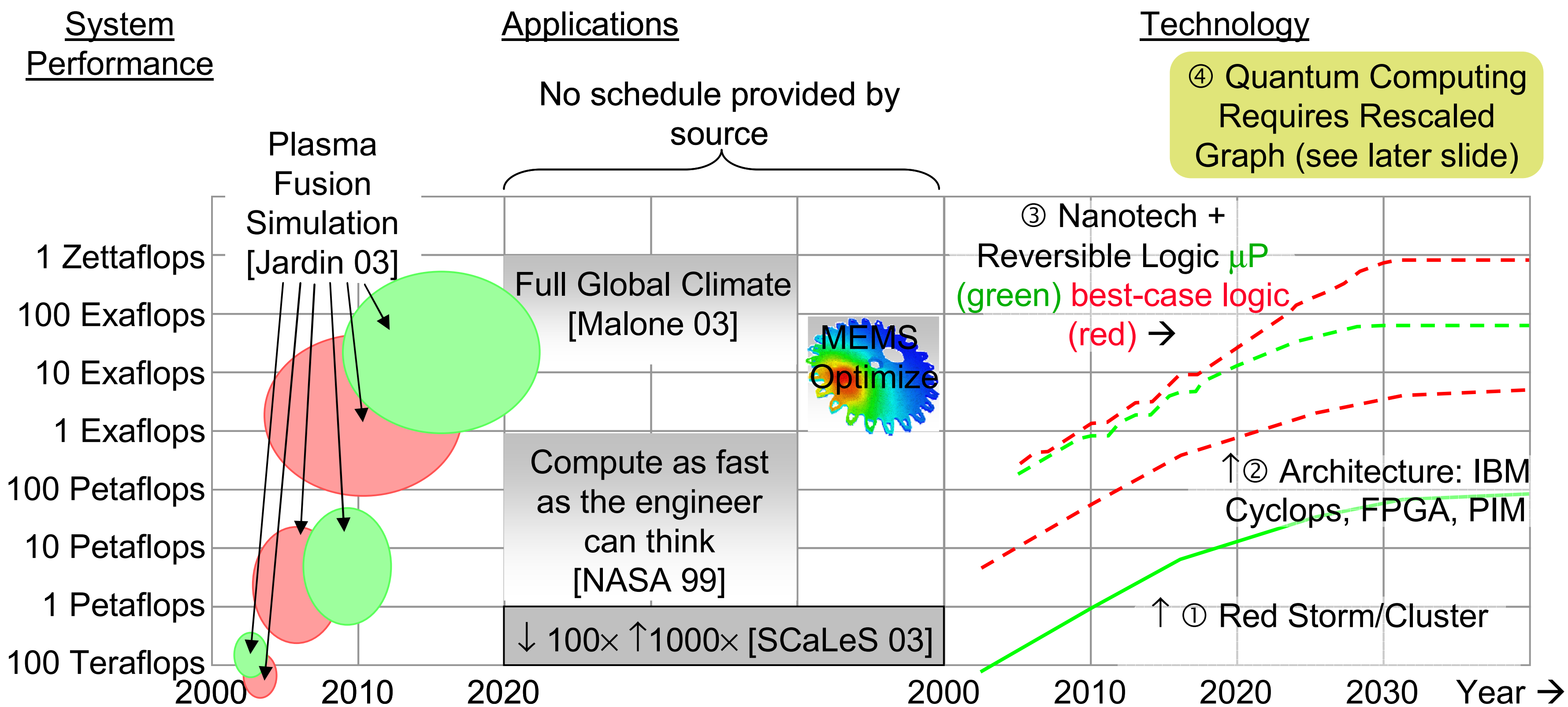
Applications and $100M Supercomputers



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[SCaLeS 03] Workshop on the Science Case for Large-scale Simulation, June 24-25, proceedings on Internet a http://www.pnl.gov/scales/.
[DeBenedictis 04], Erik P. DeBenedictis, "Matching Supercomputing to Progress in Science," July 2004. Presentation at Lawrence Berkeley National Laboratory, also published as Sandia National Laboratories SAND report SAND2004-3333P. Sandia technical reports are available by going to http://www.sandia.gov and accessing the technical library.

Experiments Under Discussion

- Continuation of Quantum Fortress work 1100
- Molecular QCA 1800
- Quantum Computing Tie-In
  - Architecture
  - Quantum Dot Measurements
  - Quantum Dot Manufacturing classical/quantum
- Computer Architecture beyond limits of Moore's Law
- Simulation of information+Physics