Superconducting Electronics and Future Computing

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ITRS Meeting on Fundamental Concepts in
Emerging Research Architectures
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Motivation

- SCE possible rollout as a low-power data center technology
  - Half-rack to data center → SCE
  - Mobile, embedded, and personal computers → CMOS
- Lessons to be learned that apply to all Beyond CMOS
  - Track behavior of interconnect
  - Track efficiency of a logic family in expressing a given function

Outline

- SuperConducting Electronics (SCE) Overview
- SCE-Compatible Memory
- Cross-device Energy Comparisons
- Architecture Lessons
  - Wiring and Interconnect
  - Function
- Sub-kT Experiments (controversial)
- Conclusions and Recommendations

Quick SuperConducting Electronics (SCE) logic overview

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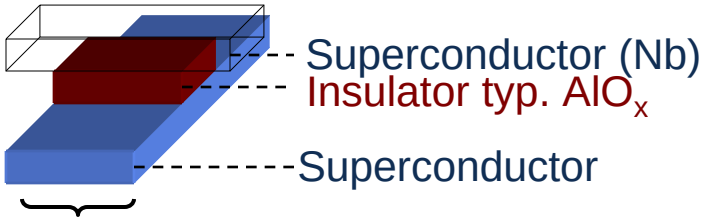
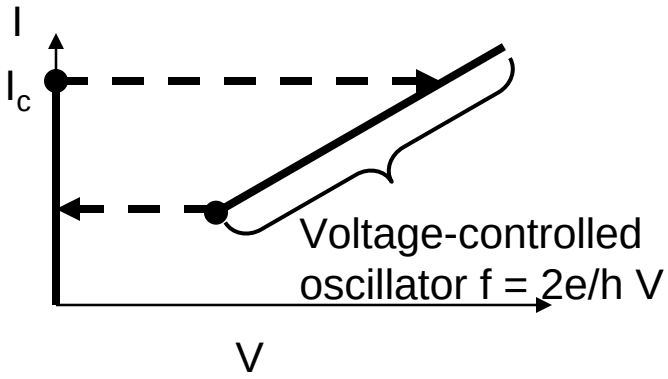
Josephson Junction (JJ) Physical:

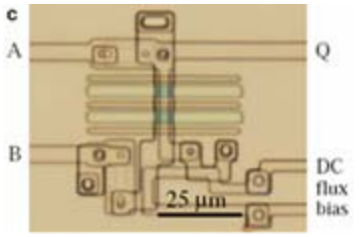


>100 nm

JJ I-V curve:



Example (RQL A and !B gate):



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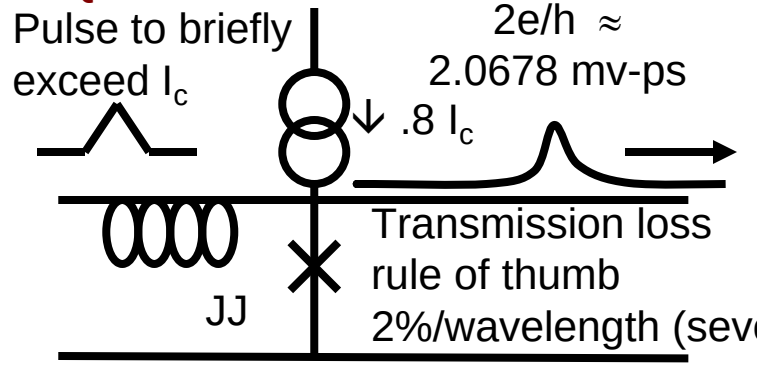
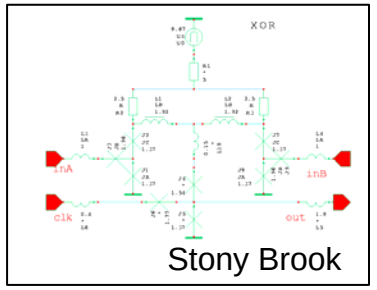
RSFQ:



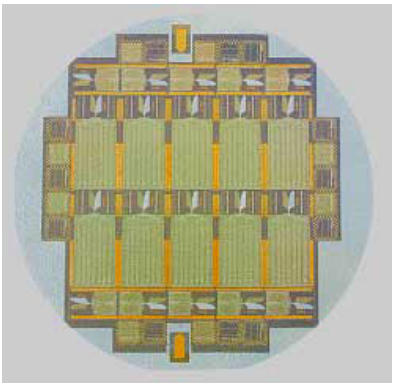
RSFQ XOR gate:



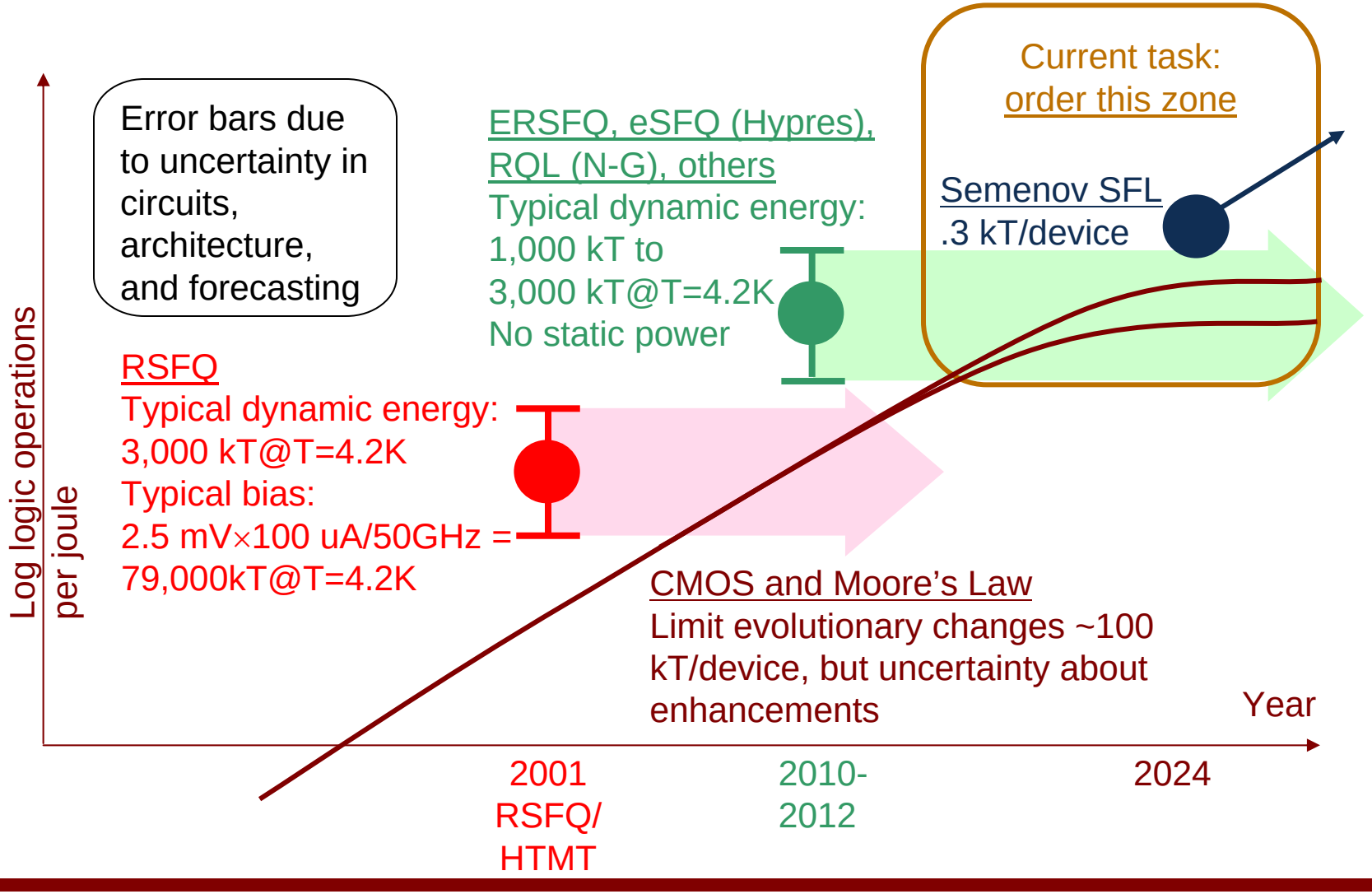
HTMT (not built):

US Government photos

Voltage standard:



SCE energy efficiency tracks Moore's Law (but the point was not considered at the time)



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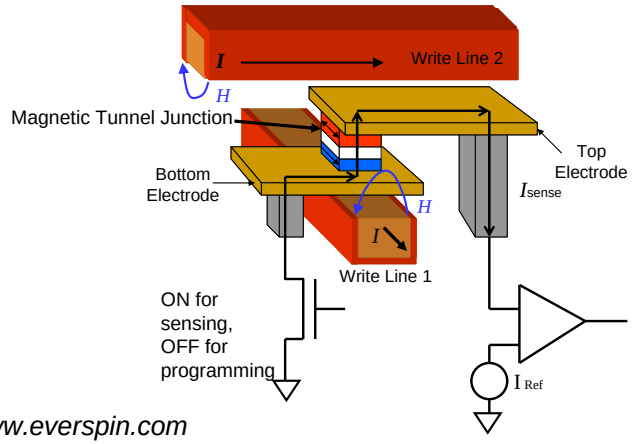
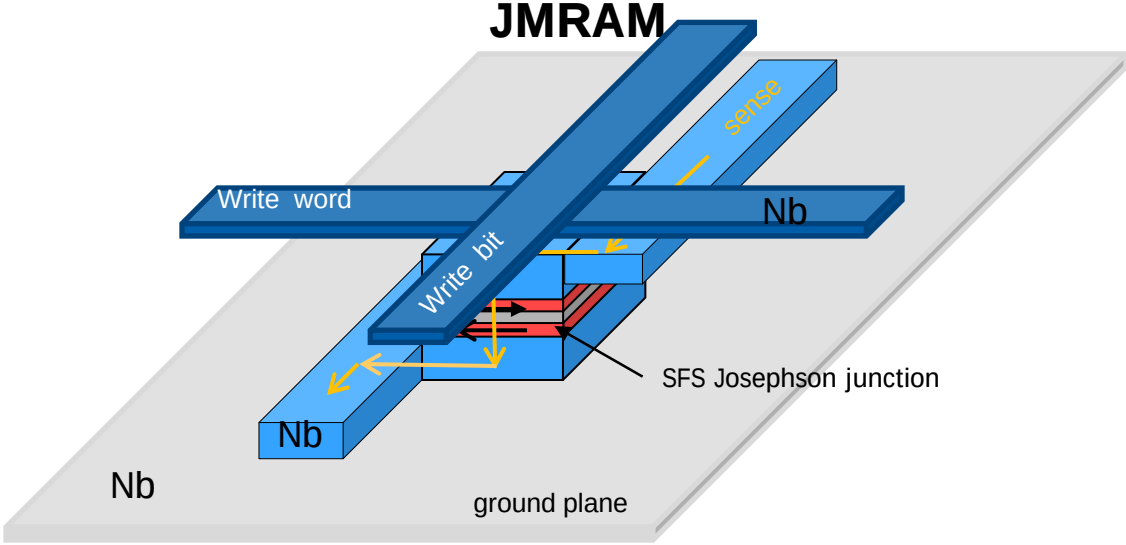
JMRAM is a superconducting MRAM

Toggle MRAM



www.everspin.com

JMRAM



Memory cell is a magnetic tunnel junction with superconducting electrodes: underlining physics demonstrated on SFS Josephson junction

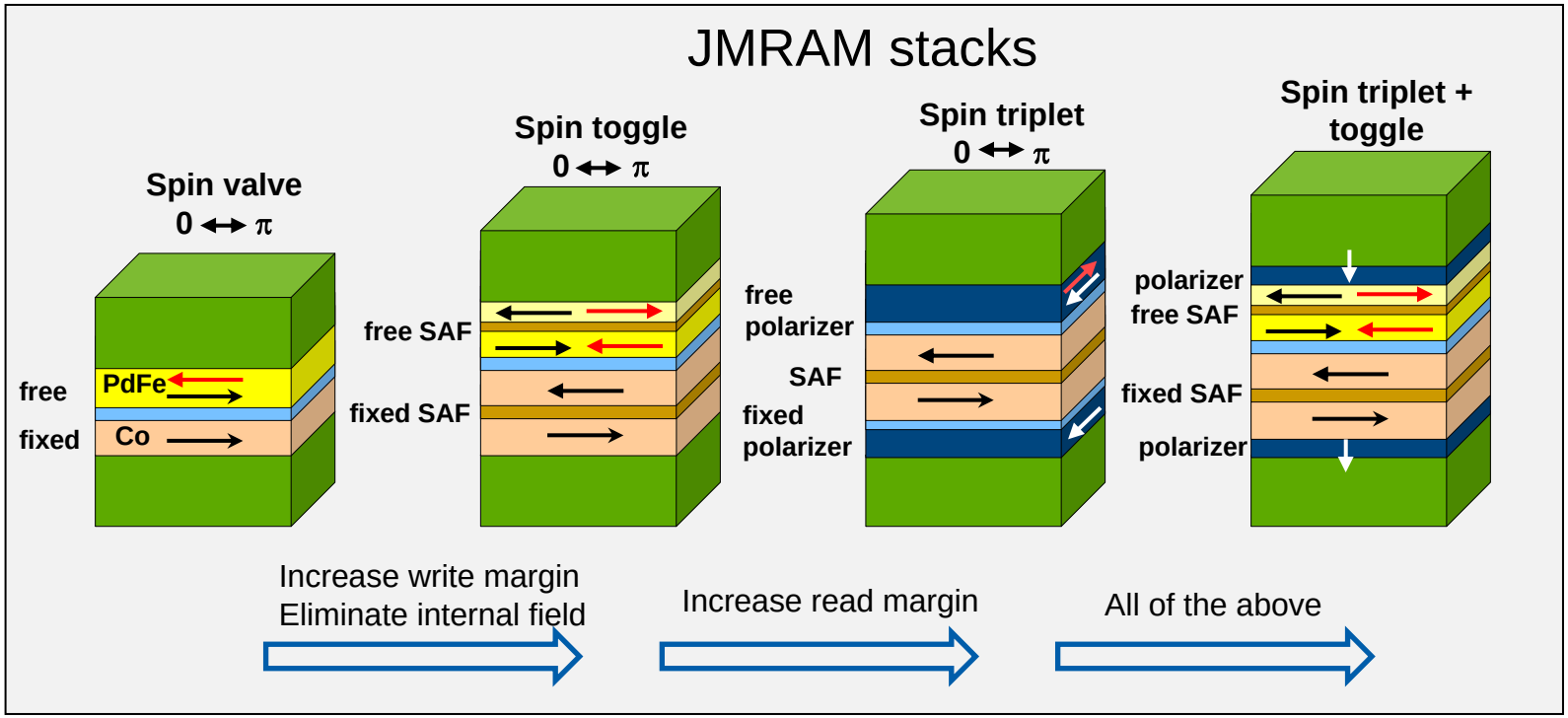
memory state – critical current magnetic hysteresis

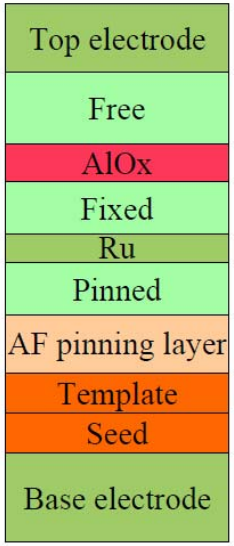
write – spin reversal

read – Josephson effect

No idle/static power dissipation, read energy is dissipated only for logical “1”

JMRAM offers dense and low-power solution for superconducting memory compatible with standard MRAM fabrication and Josephson junction processes





High density	→	two Josephson junctions per cell	→	$10^8/cm^2$
Low energy write	→	reduced switching energy at 4.2 K	→	2 fJ per bit
Ultra-low energy read	→	low energy Josephson junctions	→	2 aJ per bit
Fast access time for read	→	time-of- flight in Nb line	→	100 ps for 2Mb

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Energy efficiency of cryogenically cooled electronics

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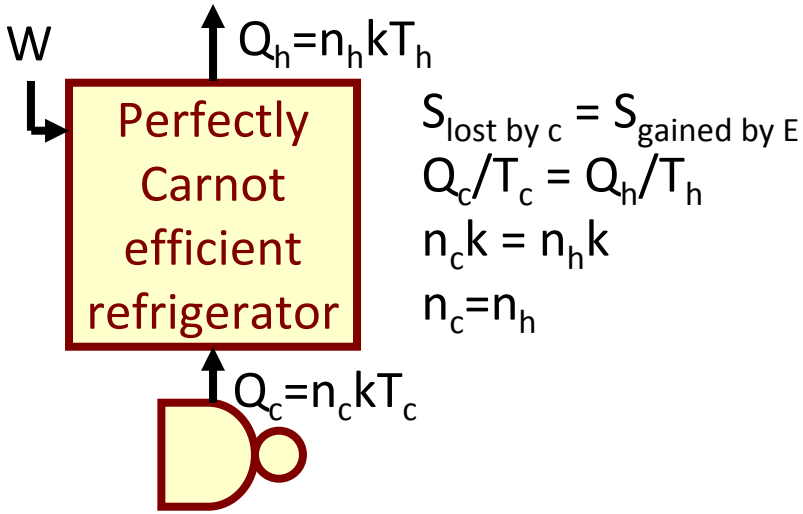
Energy strategy

- Express gate energy in units of kT; T is operating temperature
- Add overhead as "percentage of Carnot efficiency"



$S_{lost\ by\ c} = S_{gained\ by\ E}$

$Q_c/T_c = Q_h/T_h$

$n_ck = n_hk$

$n_c=n_h$

Economy of scale in cryo refrigerators

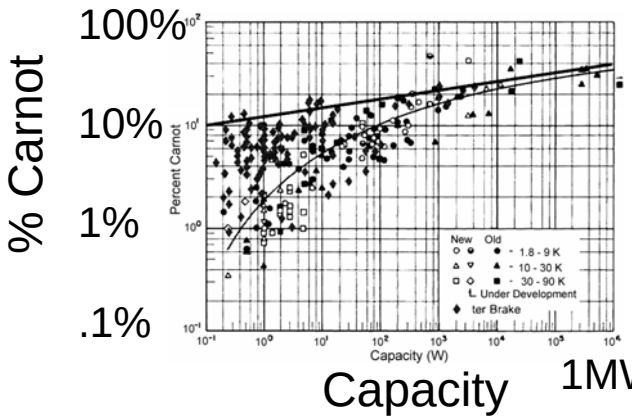


Chart from "Refrigeration for superconducting and cryogenic systems," USG not subject to copyright

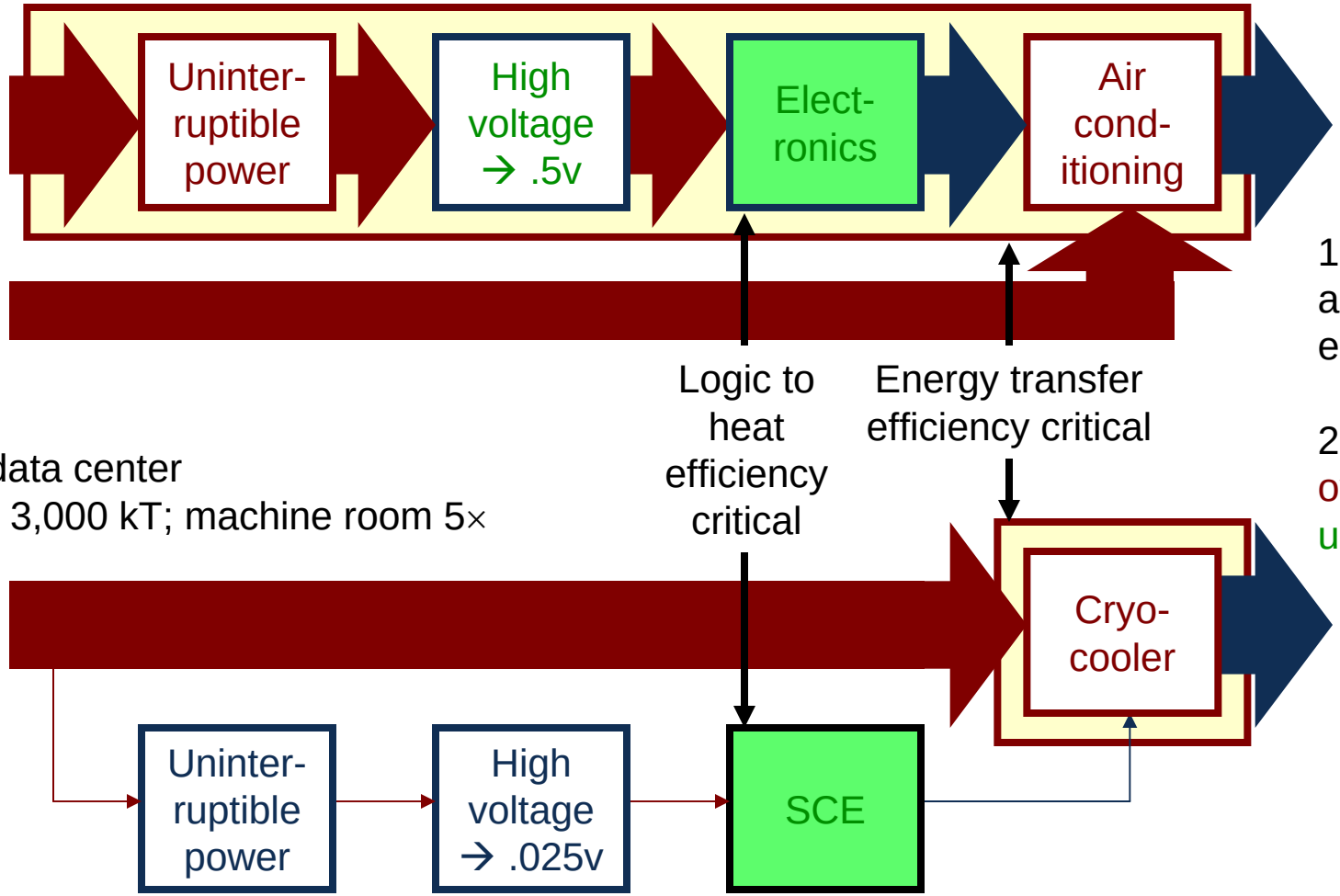
- Data center is typically 50% efficient
- Exascale refrigerator 20% Carnot
- Ratio 2.5:1

Linde website

If you measure computing in units of kT, cooling creates a penalty of 2.5× (typical) – ~4× (Google/Facebook) against superconducting electronics

Inter-device data center power efficiency model: kT/logic op + % Carnot efficiency

Current data centers:
Logic: 50,000 kT to 500,000 kT; machine room: 2× (to 1.06× Google)



1. Arrow width approximates energy transfer

2. Text color is overhead vs. useful work

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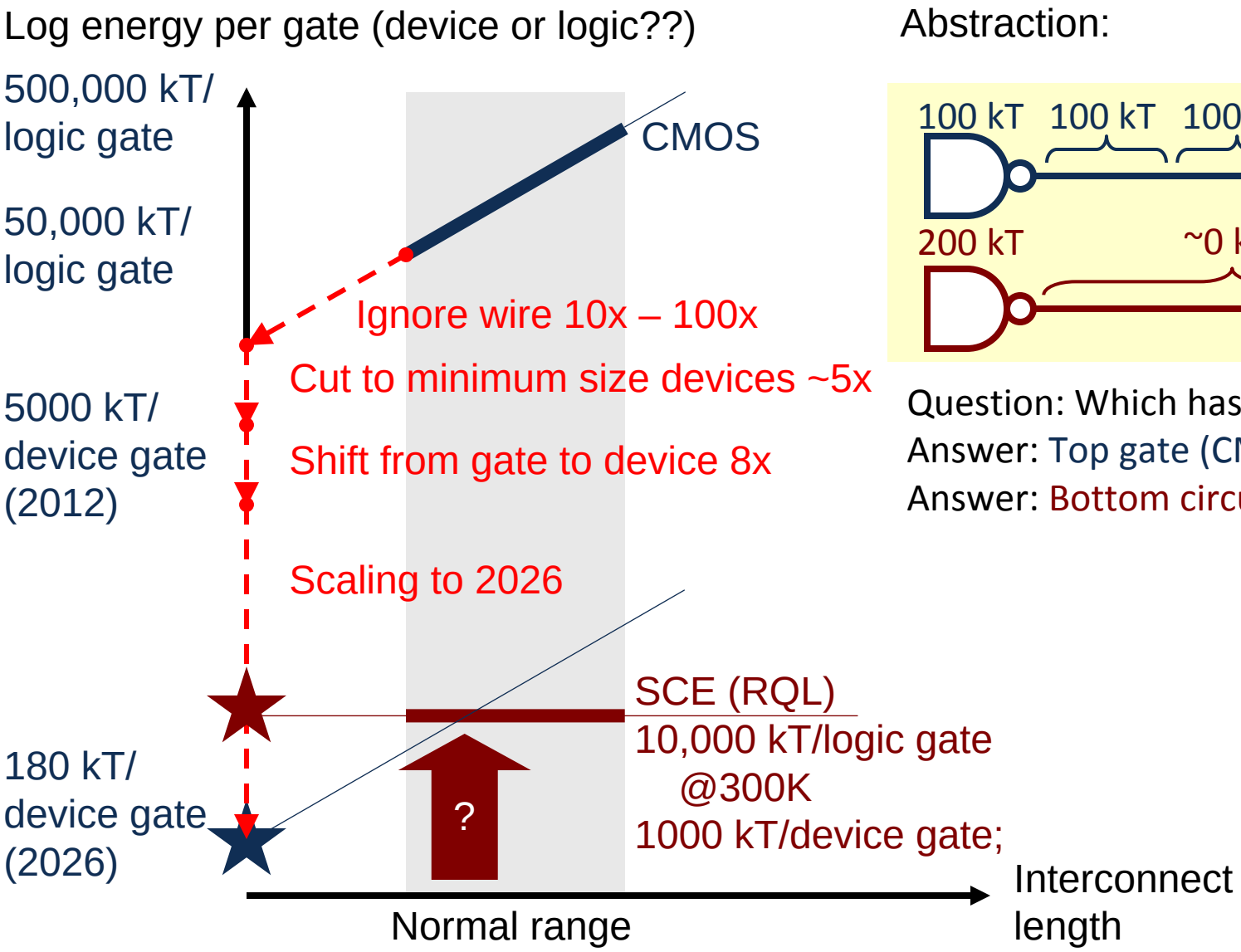
Energy accounting at the gate-and-wire level



Abstraction:

Question: Which has lower energy?

Answer: Top gate (CMOS)

Answer: Bottom circuit (SCE)

Logic energy is strongly impacted by wiring for SCE

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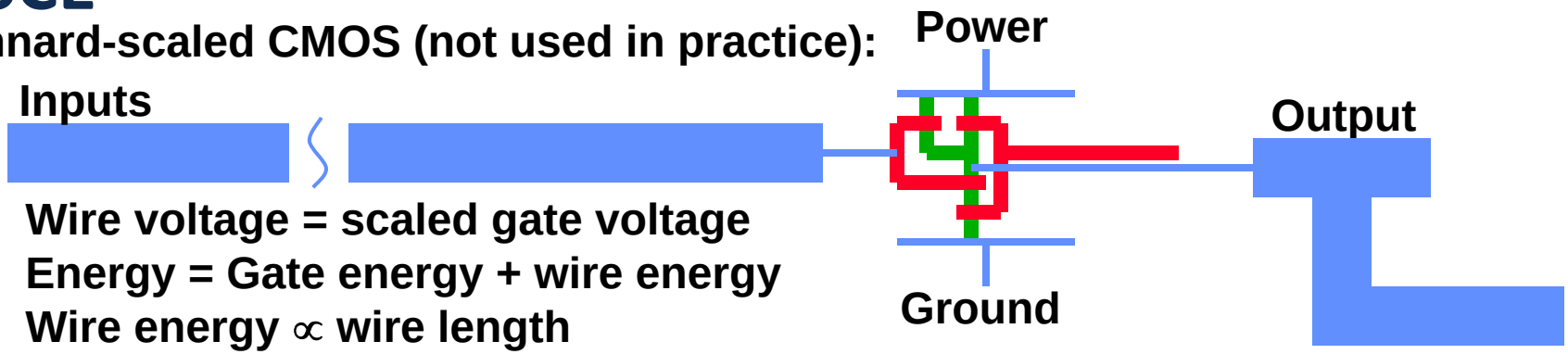
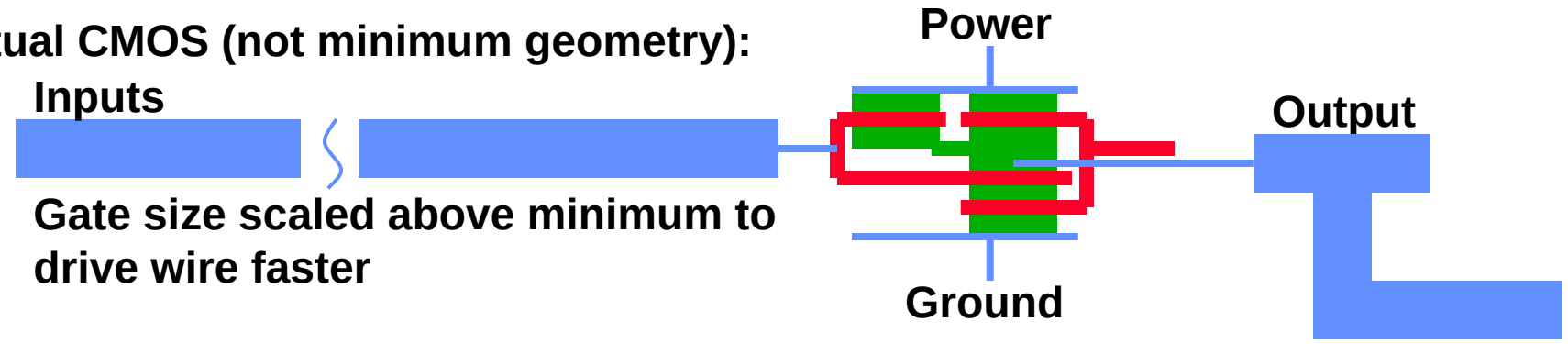
Dennard-scaled CMOS (not used in practice):



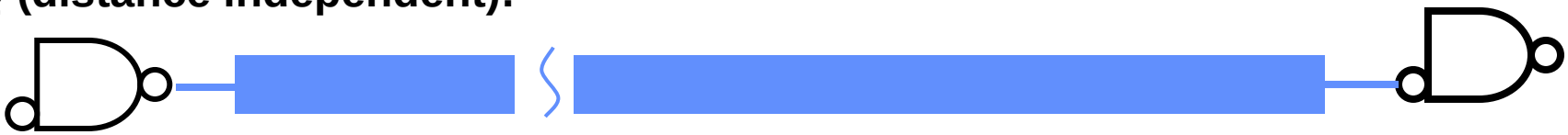
Wire voltage = scaled gate voltage
Energy = Gate energy + wire energy
Wire energy $\propto$ wire length

Actual CMOS (not minimum geometry):



Gate size scaled above minimum to drive wire faster

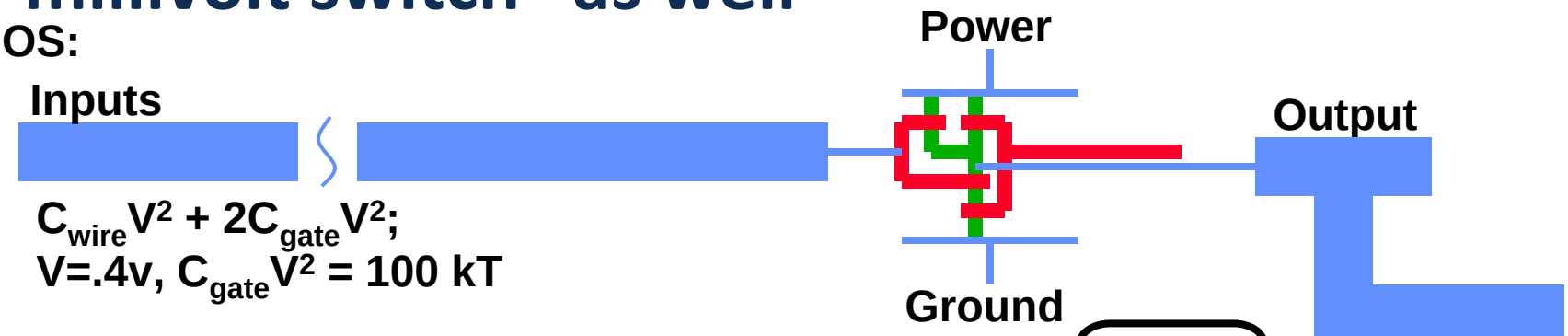
SFQ (distance independent):



SFQ pulse propagates ballistically; repeaters after several centimeters (rule of thumb: 2%/wavelength)

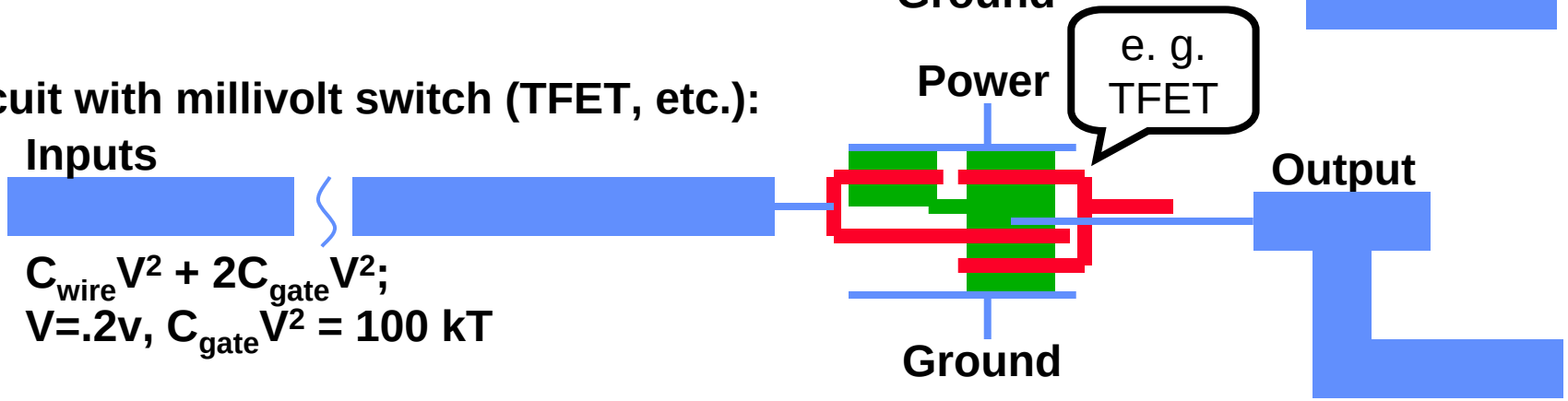
Logic energy is strongly impacted by wiring for "millivolt switch" as well

CMOS:



$C_{wire}V^2 + 2C_{gate}V^2$;
$V=.4v$, $C_{gate}V^2 = 100\ kT$

Circuit with millivolt switch (TFET, etc.):



$C_{wire}V^2 + 2C_{gate}V^2$;
$V=.2v$, $C_{gate}V^2 = 100\ kT$

Example:

1. Scale to 100 kT on gates
2. Cut supply voltage in half (now need millivolt switch)
3. Make gates 4× wider so they stay at 100 kT
4. Result: Wire energy reduced 4×; gates still at 100 kT

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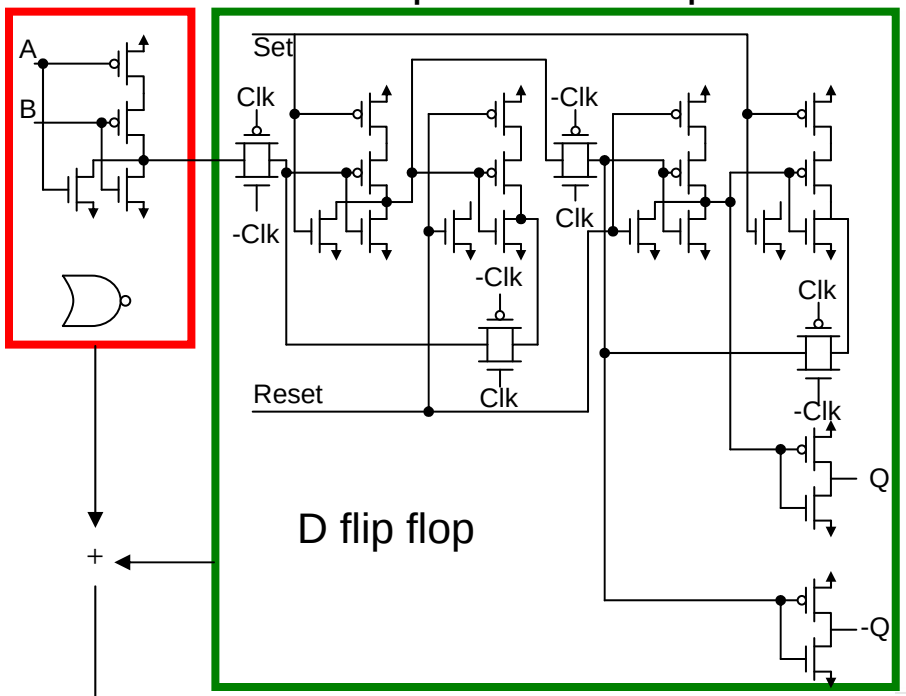
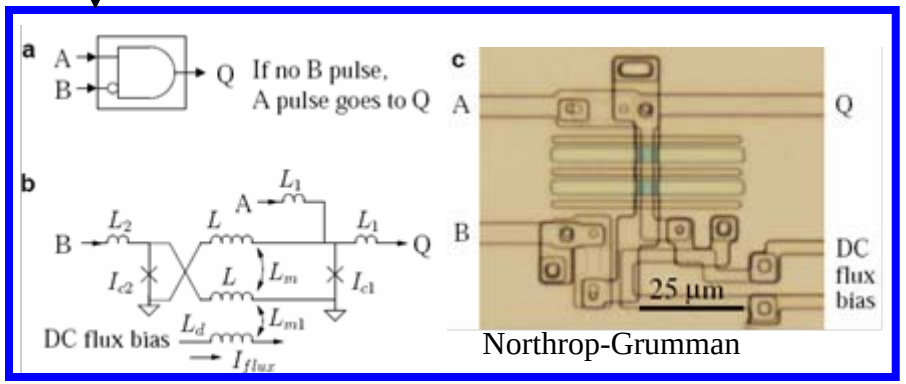
Cross-device comparison; fair function comparisons

Devices MAY not be equally useful

- In SCE design style, SCE blue is equivalent to CMOS red plus CMOS green
- Many SCE gates have a latch on output, which is hard to remove
- Accommodations
  - Handicaps for device utility
  - New design tools

Function correspondence imprecise!





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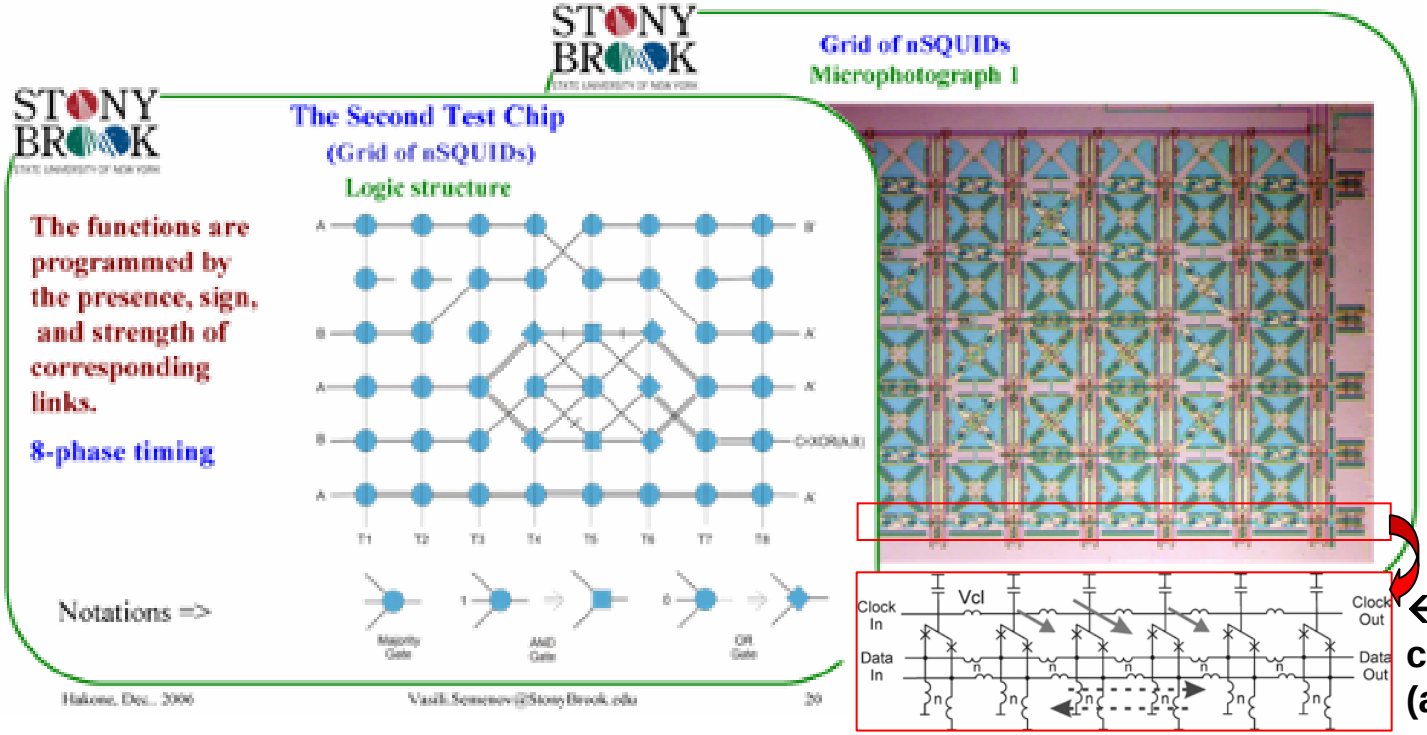
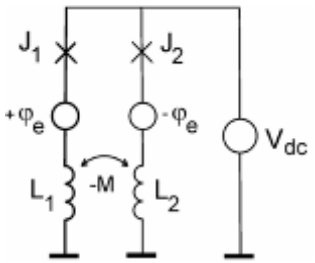
Sub-kT experiments on low power computing

- **Reversible logic family**
  - Left is logic design method
  - Right is a photomicrograph
    - NOT DEBUGGED

- **Key Features**
  - Superconducting transmission lines are nearly lossless
  - Uses recovery and recycling of signal energy



nSQUID (-M negative inductance):



← Energy recycling clock/power supply (aligned to chip photograph)

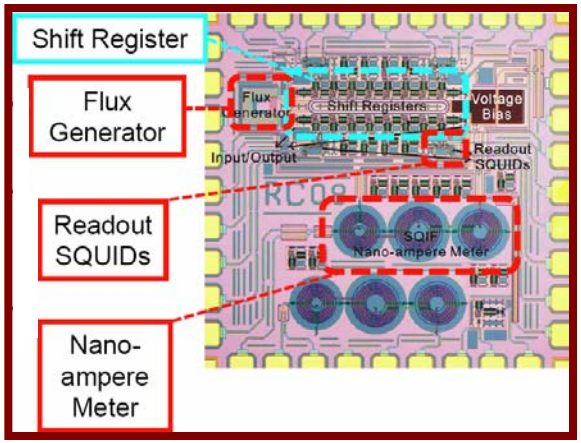
V. Semenov, Stony Brook (refs detailed in PowerPoint notes)

Significance of sub-kT computing

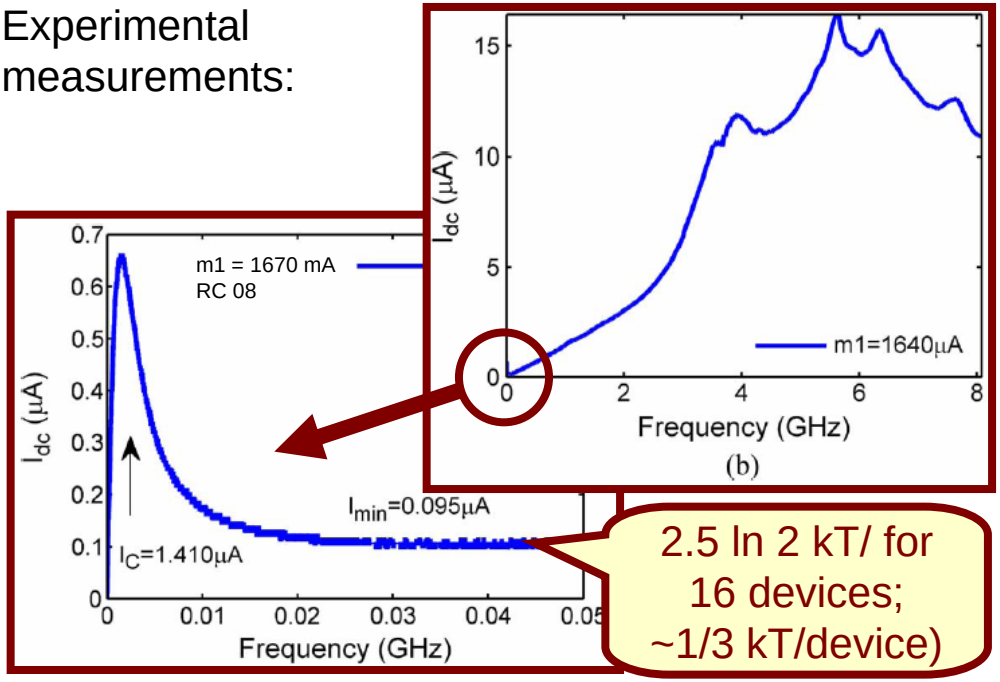
- Since the 1940s, information technology has grown exponentially, and is now a major industry
- Society would change if computer growth stopped
- How long with it continue?
  - 100 kT/logic op?
  - .7 kT/logic op?
  - Lower?
- Sub-kT roadmap entry?
  - Has been impossible to demonstrate experimentally
  - Maybe time for yellow entry?

Test circuit RC08:

Source: Progress With Physically and Logically Reversible Superconducting Digital Circuits, Jie Ren and Vasili Semenov, IEEE Transactions on Applied Superconductivity, June 2011



Experimental measurements:



2.5 ln 2 kT/ for 16 devices; ~1/3 kT/device)

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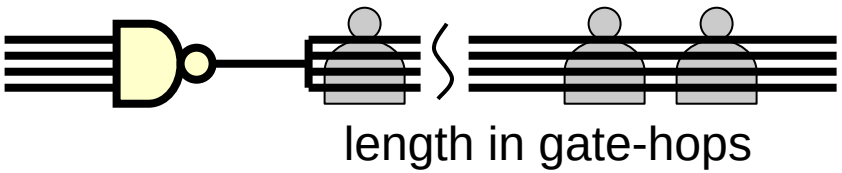
Conclusions

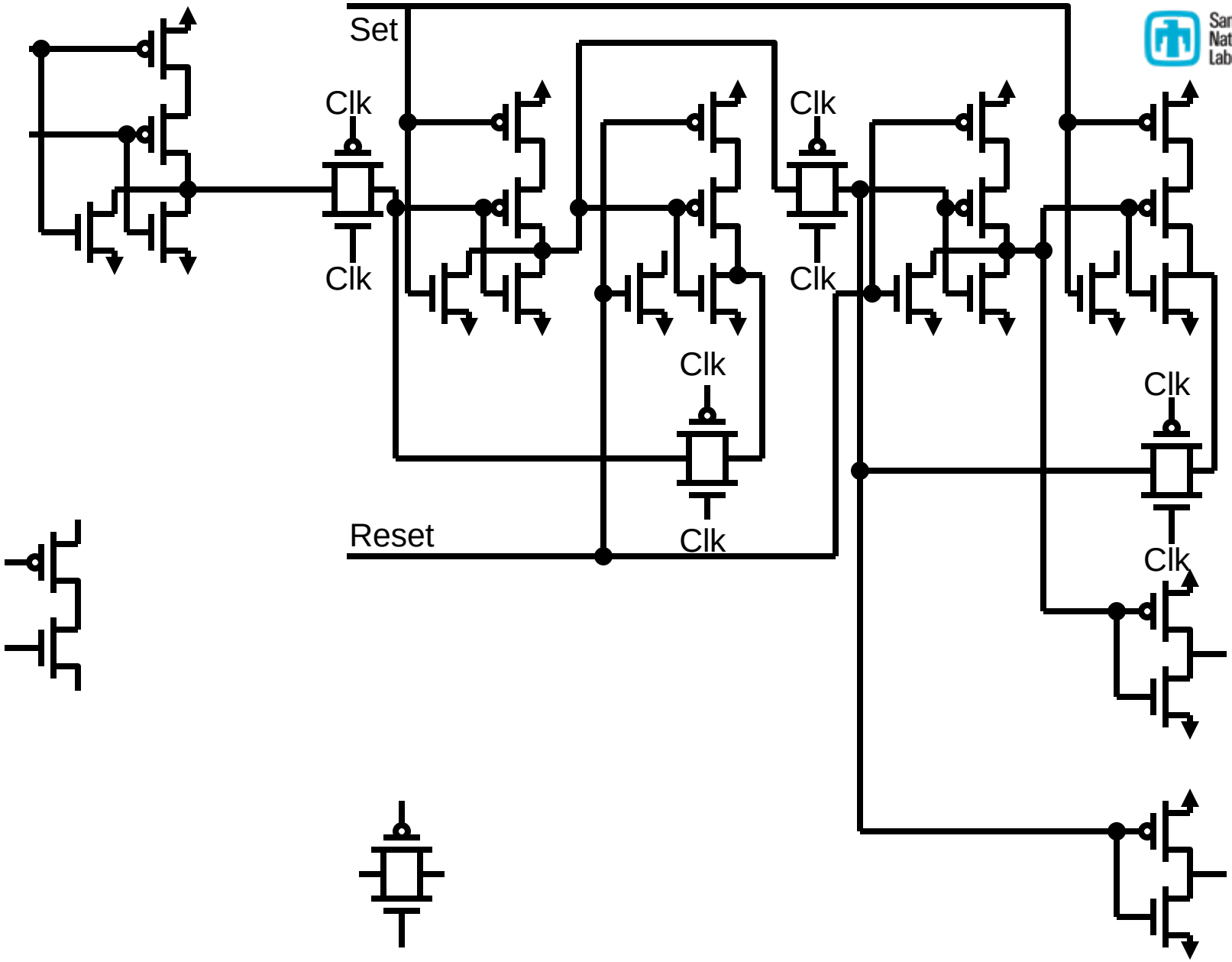
- The small SCE industry has tracked CMOS's energy efficiency
  - RSFQ (equivalent of ECL) has been notable historically
  - Modern SFQ derivatives can be compared to CMOS at the projected end of CMOS scaling
- Proceeding forward
  - SCE's future implies market segmentation (mobile + data center)
  - SCE provides lessons for inter-device comparisons
    - Recommendation 1: Energy efficiency needs to be measured differently
    - Recommendation 2: Interconnect wire must be considered
    - Recommendation 3: Logic functions differ in value to circuits, which should impact energy efficiency
  - SCE memory research needs to be successful
  - Demonstrations of sub kT logic appear to be imminent (red→yellow?)

General recommendations for Beyond CMOS devices

- Consistent energy ratings
  - Express logic energy in units of kT (i. e. entropy)
  - Account for data center energy losses as a burden on the device
- Wire
  - Develop a model for “logic + interconnect wire” overhead
    - wire length depends on architecture (e. g. short, medium, long wires)
  - This will prevent “gaming the system” by creating logic devices that produce signals that are hard to move around



- Logic
  - The efficiency with which a logic family can realize functions needs to be captured and can become an energy handicap on the device


Set
Clk
Clk
Clk
Clk
Clk
Clk
Clk
Clk
Reset